BIST Implementation For Testing Analog Circuit In Mixed Signal Environment

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Abstract: This Paper aims to develop approaches to test Analog & Mixed signal circuits with build in hardware. In this paper we study various methodologies for testing analog component in Mixed Signal Circuits. We studied various methodologies like Simple BIST Structure, OBIST, DDS (Direct digital Synthesizer using BIST or Automatic Generation of BIST.

We present a software method for automatic generation of digital circuitry for testing & synthesis. Here BIST circuitry includes frequency response (both gain & phase) linearity & noise figure.

The oscillation-based built-in self-test (OBIST) methodology proposes the structure utilized for on-chip generation of oscillatory responses corresponding to the analog-circuit components.

Key Words: BIST, OBIST, DDS (Direct digital Synthesizer using BIST), response compaction unit (RCU,) Design For Testability (DFT), Integrated Circuit (IC), Circuit Under Test (CUT),Test Pattern Generator (TPG).

1.INTRODUCTION:

Due to increasing complexity and decreasing physical size of electronic circuits and systems implicate the necessity of developing new methods and techniques of their testing and fault diagnosis. One of the important methed of development of the testing and diagnostic technique of electronic systems is the built-in self-test (BIST) technique [1]. It is characterized by the ability to identify the condition of system operation by itself through the testing and diagnosis capabilities built into its own structure of the system.

An approach to developing test strategies for analog circuits in mixed-signal embedded core- based SOC environments based on oscillation-based BIST (OBIST) [1] architecture is investigated. In the process, the technique for modifying a given circuit so as to make it testable is discussed based on the principles of OBIST methodology [2-6].

An important objective to realize through detailed testing is to ensure that the manufactured products are free from defects and to simultaneously guarantee that they meet all the required specifications. Besides, the Information that may be acquired through the process may ultimately help in increasing the product yield, thereby reducing the product cost. The integrated-circuit (IC) fabrication process involves photolithography, printing, etching, and doping steps.

Recently, none of these steps is ever perfect, and the resulting imperfections may eventually lead to failures in the operation of the individual ICs. Specifically, the performance of mixed-signal ICs will be greatly degraded, since these circuits are very sensitive to even small imperfections in any step of the fabrication process.

For development in analog and mixed signal circuits domain, now a time we are implanting BIST methods for testing analog and mixed signal circuits.

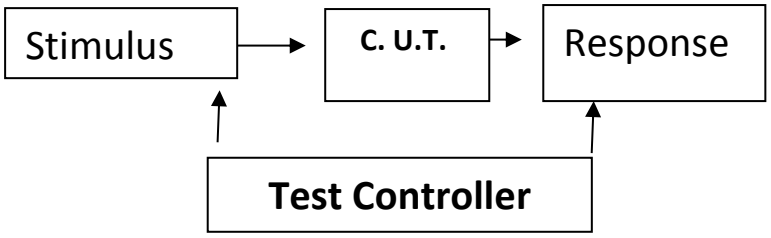

Fig. 1 Typical BIST structure

A typical BIST environment, as shown in Fig. 1, uses a test-pattern generator (TPG—stimulus source) that sends its outputs to a circuit under test (CUT), and output streams from the CUT are fed into a test data analyzer. A fault is detected if the test sequence is different from the response of the fault-free circuit. The test data analyzer is comprised of a response compaction unit (RCU), storage for the fault-free responses of the CUT, and comparator [7].

2. METHODOLOGIES:

OBIST

The test methods for analog and mixed signal circuits are based on rearranging the CUT to an oscillator.

For test of complex mixed-signal systems designed in nanotechnologies, standard test methods cannot be straight forwardly used because of the poor testability of such systems and unrealistic requirements for capabilities of ATE (Automatic Test Equipment) [7]. Therefore, development of new test strategies and approaches represents an important task and challenging issue towards reliability enhancement of complex integrated systems. Parametric test methods are most commonly used for testing of analog and mixed-signal ICs. These methods are based on the monitoring of a specific circuits parameter such as voltage, supply current, frequency, etc. Parametric test is usually rather difficult (in comparison to logic test) because it requires sophisticated sensing, measurement and evaluation of the selected parameter, setting the Pass/Fail limit, test hardware robustness, etc. [8].

The fault is revealed from a deviation of its oscillation parameters with reference to the parameters below the fault free conditions. The oscillation parameters are freelance of the CUT type and analog testing. The block diagram of OBIST strategy is illustrated in figure (3).

The testing techniques for analog & mixed signal circuits are based on rearranging the CUT to an oscillator. During this technique the complicated analog circuits are divided into various building block like Schmitt trigger, voltage reference, oscillator, OP-AMP,PLL or combination of all these blocks.

During the test mode, each building block of circuit is converted into an oscillator by adding the proper circuitry in order to achieve sustained oscillation. The oscillation is then evaluated [8-10].

The application of testing procedure is proposed in this paper. Catastrophic faults (stack open and stack short) are injected into the CUT. These faults after being injected into the nominal circuit descriptions by using the simulator, evaluates the transient response while frequency and output voltage are measured. The fault free circuit is converted into an oscillator and simulated and its test parameter is thus derived. The different steps of the procedure are briefly given in fig.3.

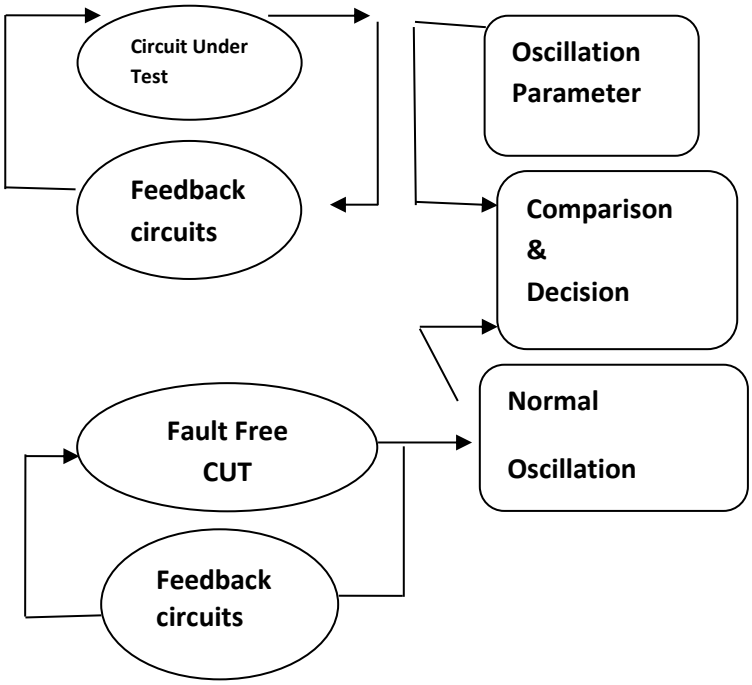

Fig. 2 OBIST structure

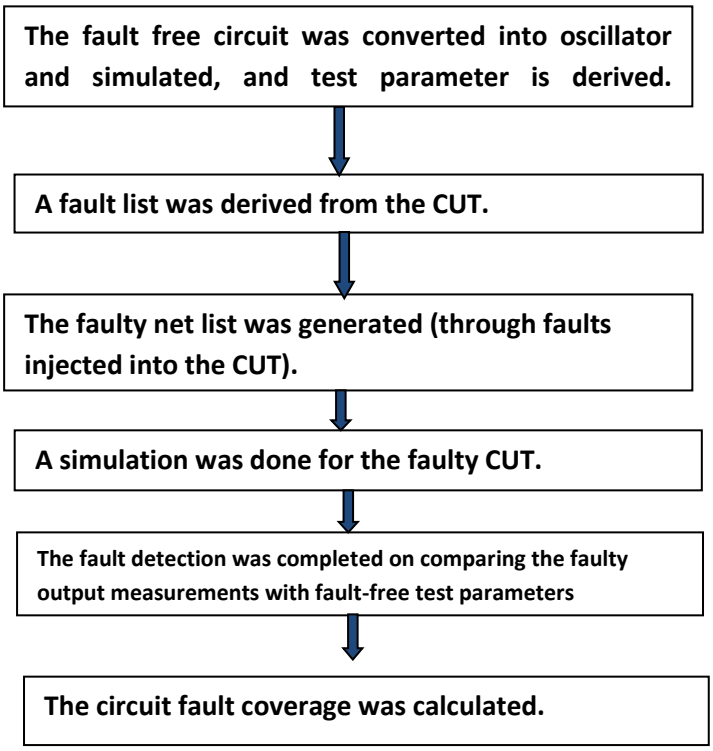

Fig. 3 Fault testing procedure

AUTOMATIC GENERATION OF BIST

The majority part of the BIST circuitry resides in the digital portion of a mixed-signal system and includes a direct digital synthesizer (DDS) based test pattern generator (TPG), a multiplier/accumulator (MAC) based output response analyzer (ORA), and a test controller. The only test circuitry added to the analog domain is one or more analog loop back paths to facilitate direct measurement of the test signals by the ORA. The number and location of these loopback capabilities determines the accuracy and resolution of tests and measurements associated with a given analog circuit. For implementing this approach first of all we compare the synthesized circuit on the field-programmable gate-array (FPGA) technology. We have been investigating and analyzing this DDS-based BIST approach for its ability to detect faults and to assist in characterization and calibration during manufacturing and field testing.

we analyzed a potential problem with the BIST approach is that the ORA faces the phase delays which distort the gain measurement in the frequency response test. This is also a concern during the linearity test near the cutoff frequency. However, we will show that a simple measurement made with the existing hardware of the BIST approach can determine the actual phase delay. This allows us to not only measure the phase delay of a circuit, but also to correct the measured gain and linearity. The proposed BIST scheme, using the existing ADC/DAC, will automatically meet the system dynamic range requirement which fully demonstrates the fidelity of the proposed BIST approach for analog linearity and frequency response tests [12-16].

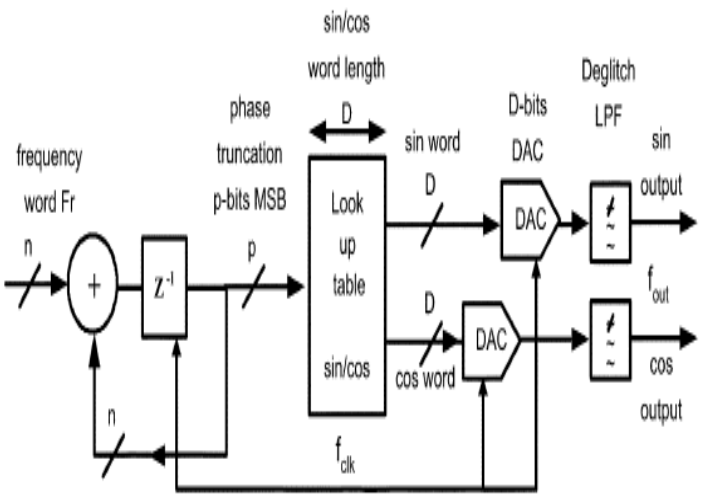

Fig.4 DDS for test-signal generation.

In this method we studied a BIST approach for analog circuit functional testing measurement of amplifier linearity and frequency response including

both phase and gain. The DDS-based TPG is used to generate two frequency tones required in the two-tone linearity test, as well as single tones for frequency response measurements. The efficient ORA consisting of a multiplier and accumulator, avoids using traditional FFT-based spectrum analysis which consumes much more power and die area.

An very important frequency synthesis technique known as DDS, which provides low-cost synthesis with ultra-fine resolution. As shown in Fig. 4, a conventional DDS includes a digital accumulator that generates the phase word based on the input frequency word Fr, where Fr determines the output frequency as Fout = $(Fr/2^2)$,f_{clk}. The synthesizer step size is defined as, $f_{clk}/2^n$ where n is the number of bits in the accumulator. By large accumulator size fine resolution can be achieved. . In DDS technique lookup table converts the phase word to a sinusoidal amplitude word, whose length is normally limited by the finite number of input bits of the DAC. Deglitch filters are added after the DAC to remove the spurious components generated in the data conversion process. While a pure sinusoidal waveform is desired at the DDS output, spurious tones can occur mainly due to the following two nonlinear processes.

First, in order to reduce the lookup table ROM size, the phase word needs to be truncated before being used as the ROM addresses. This truncation process introduces quantization noise, which can be modeled as a linear additive noise to the phase of the sinusoidal wave. Second, the ROM word length is normally limited by the finite number of bits of the available DAC. In other words, the sinusoidal waveform can be expressed only by words with finite length, which intrinsically contains quantization error additive to the output amplitude. Considering the quantization errors due to phase truncation E_P, and finite amplitude resolution E_A, and assuming the phase quantization error is small relative to the phase, the DDS output can be determined as

$$\mathbf{B_{out} = A \sin\ [2\pi\ W_i / 2^n\ + E_p(i)]+ E_A(i)}$$

$$B_{out} = A \sin(2\pi W_i/2^n) + A E_P(i) \cos(2\pi W_i/2^n) + A E_{A\,i}(i) . \quad (1)$$

Table1.Comparative Study of various BIST techniques

Comparative Study of various BIST techniques				
Name of Authors	**Year of Publication**	**Name of techniques**	**Testing Parameter**	**Remarks**
M. F. Toner, G.W. Robert	1993	MADBIST	An SNR Test	For ADC Circuit
Karim Arabi, Bozena Kaminska	1999	Oscillation technique	Oscillation	For active analog filter
Nicola Nicolici, Bashir M., Al-Hashimi, Andrew D. Brown, Alan C. Williams	2000	BIST Hardware	TCCs	For RTL Circuit
Robert X. Gao	2005	Embedded based Test system	Jitter Measurement	Hardware testing of SOC
Sunil R. Das	2006	Self testing With BIT	TPG	Testing of VLSI circuit
Foster Fa Dai	2006	BIST based on DDS	Frequency Response	BIST on FPGA
George J. Starr,Jie Qin , Bradley F. Dutton, Charles E. Stroud	2009	DDS based TPG	Frequency, phase	Easy to Implement
Hao-Chiao Hong, Fang –Yi Su , Shao-Feng Hung	2010	Fully integrated BIST	SNDR, Offset, Gain Error	AUT The ADC under test
Dariusz Załe¸ski, Romuald Zielonko	2010	CS-BIST	Testing analog circuit	Testing of forth order filter
Mradul Kumar Ojha, Shyam Akashe	2015	OBIST	Functional & Structural Testing	Inverter, Oscillator circuit

3. CONCLUSION

Hence we studied various BIST methods for testing analog and mixed signal circuits. Here we firstly studied basic structure of BIST method. This paper also investigates method of OBIST technique in testing analog parts in mixed-signal circuits. The OBIST method does not require stimulus generators or Complex-response analyzers and has been gainfully employed in testing analog and mixed signal circuit in embedded core based SOC environment.

Here in paper we also approached the DDS-based TPG which is used to generate two frequency tones required in the two-tone linearity test, as well as single tones for frequency response measurements.

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