Design of Image by Morphological Dilation Technique using Xilinx tool on FPGA

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Abstract: Mathematical morphology is a well known image and signal processing technique. However, most morphological tools such Matlab are not suited for strong real-time constraints. We address this problem through hardware implementation on FPGAs. This paper gives the algorithm and implementation of morphological image processing on FPGA. The design is implemented on a Xilinx xc3s500e-4fg320 FPGA chip. The design is tailored to exploit certain features of sliding windows.

Keywords: Morphology, Matlab, FPGAs, Image Processing, xc3s500e-4fg320.

1. INTRODUCTION:

DIGITAL image processing is an ever expanding and dynamic area with applications reaching out into our everyday life such as medicine, space exploration, surveillance, authentication, automated industry inspection and many more areas. Applications such as these involve different processes like image enhancement and object detection. Implementing such applications on a general purpose computer can be easier, but not very time efficient due to additional constraints on memory and other peripheral devices.

Application specific hardware implementation offers much greater speed than a software implementation. With advances in the VLSI (Very Large Scale Integrated) technology hardware implementation has become an attractive alternative. Implementing complex computation tasks on hardware and by exploiting parallelism and pipelining in algorithms yield significant reduction in execution times.

There are two types of technologies available for hardware design. Full custom hardware design also called as Application Specific Integrated Circuits (ASIC) and semi custom hardware device, which are programmable devices like Digital signal processors (DSPs) and Field Programmable Gate Arrays (FPGA's).

Full custom ASIC design offers highest performance, but the complexity and the cost associated with the design is very high. The ASIC design cannot be changed and the design time is also very high. ASIC designs are used in high volume commercial applications.

In addition, during design fabrication the presence of a single error renders the chip useless. DSPs are a class of hardware devices that fall somewhere between an ASIC and a PC in terms of the performance and the design complexity.

DSPs are specialized microprocessors, typically programmed in C, or with assembly code for improved performance. It is well suited to extremely complex math intensive tasks such as image processing. Knowledge of hardware design is still required, but the learning curve is much lower than other design choices .

Field Programmable Gate Arrays are reconfigurable devices. Hardware design techniques such as parallelism and pipelining techniques can be developed on a FPGA, which is not possible in dedicated DSP designs. Implementing image processing algorithms on reconfigurable hardware minimizes the time-to-market cost, enables rapid prototyping of complex algorithms and simplifies debugging and verification. Therefore, FPGAs are an ideal choice for implementation of real time image processing algorithms.

FPGAs have traditionally been configured by hardware engineers using a Hardware Design Language (HDL). The two principal languages used are Verilog HDL (Verilog) and Very High Speed Integrated Circuits (VHSIC) HDL (VHDL) which allows designers to design at various levels of abstraction.

Given the importance of digital image processing and the significance of their implementations on hardware to achieve better performance, this work addresses implementation of image processing algorithms like median filter, orphological, convolution and smoothing operation and edge detection on FPGA using VHDL language. Also novel architectures for the above mentioned image processing algorithms have been proposed. Gray-level images are very common in image processing. These types of images use eight bits to code each pixel value, which results in 256 different possible shades of grey, ranging from 0 (black value) to 255 (white value). Latest generations FPGAs compute more than 160 billion multiplication and accumulation (MAC) operations per second.

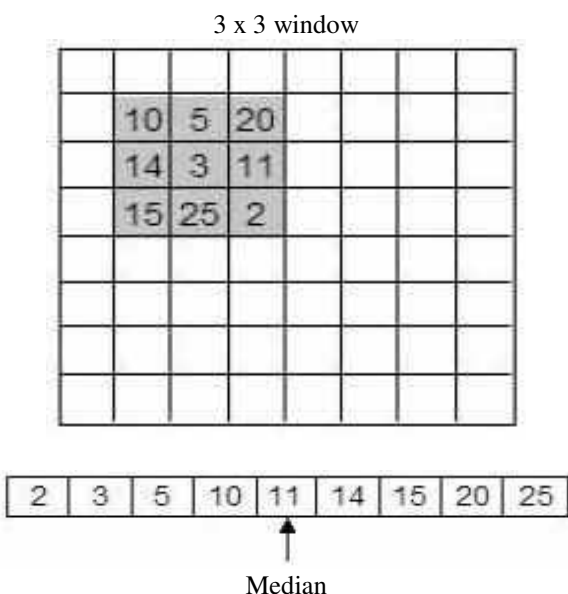## 2. IMAGE PROCESSING ALGORITHM:

This section discusses the theory of most commonly used image processing algorithms like (1) Filtering, (2) Morphological operations

A. Median Filtering: A median filter is a non-linear digital filter which is able to preserve sharp signal changes and is very effective in removing impulse noise

(or salt and pepper noise). An impulse noise has a gray level with higher or lower value that is different from the neighborhood point.

Linear filters don't have ability to remove this type of noise without affecting the distinguishing characteristics of the signal. Median filters have remarkable advantages over linear filters for this particular type of noise. Therefore median filter is very widely used in digital signal and image/video processing applications.

A standard median operation is implemented by sliding a window of odd size (*e.g.* 3x3 window) over an image. At each window position, the sampled values of signal or image are sorted, and the median value of the samples replaces the sample in the center of the window as shown in Figure1.

3 x 3 window

Median

B. Morphological Operation

The term morphological image processing refers to a class of algorithms that transforms the geometric structure of an image.

Morphology can be used on binary and gray scale images, and is useful in many areas of image processing,
such as skeletonization, edge detection, restoration and texture analysis.

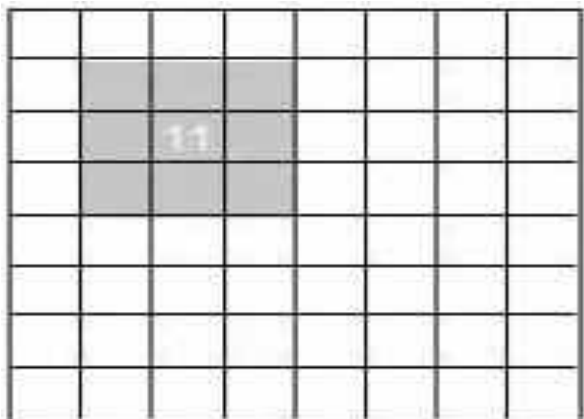Centre pixel replaced with median value
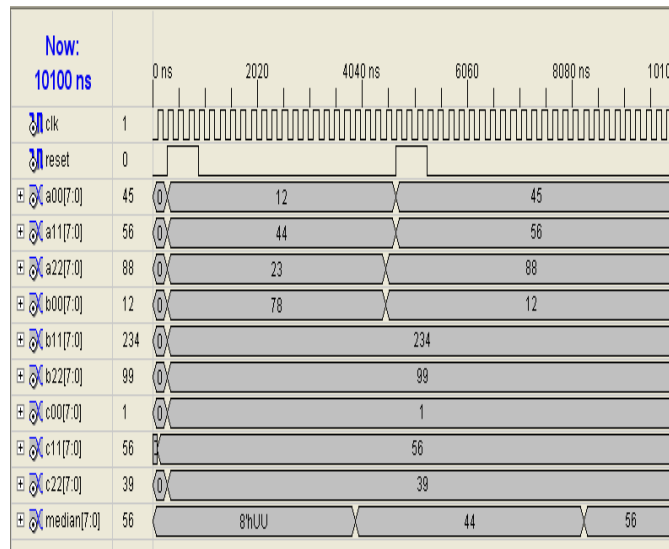

Figure 1. Median Filter.

Figure 2. Simulation result of median Filter.

The most basic morphological operations are dilation and erosion. Dilation adds pixels to the boundaries of objects in an image, while erosion removes pixels on object boundaries. The number of pixels added or removed from the objects in an image depends on the size and shape of the *structuring element* used to process the image.

 In the morphological dilation and erosion operations, the state of any given pixel in the output image is determined by applying a rule to the corresponding pixel and its neighbors in the input image.

Rules for Dilation and Erosion: Dilation- The value of the output pixel is the maximum value of all the pixels in the input pixel's neighborhood. In a binary image, if any of the pixels is set to the value 1, the output pixel is set to 1.

Erosion- The value of the output pixel is the minimum value of all the pixels in the input pixel's neighborhood. In a binary image, if any of the pixels is set to 0, the output pixel is set to 0.

The grayscale erosion is performed by minimum filter, whereas the dilation is performed by maximum filter. In a 3 x 3 minimum filter, the centre pixel is replaced by a minimum
value of the pixels in the window. In a maximum filter, the centre pixel is replaced y a maximum value of the pixels in the window. The implementation of minimum and maximum filters is similar to the median filters implementation.

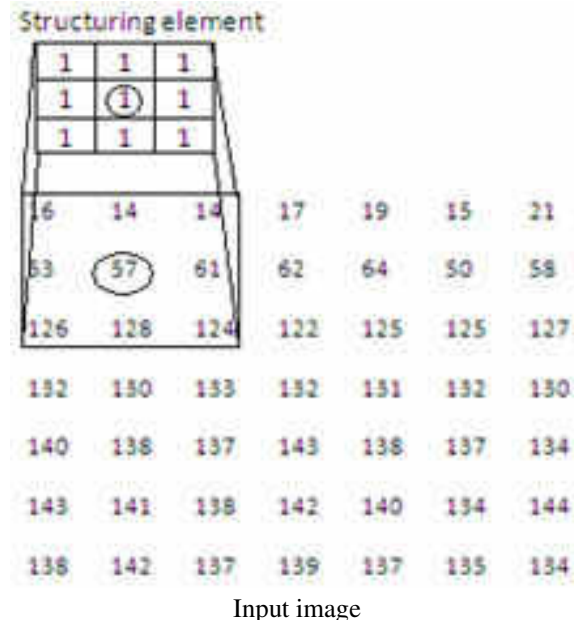Morphological Dilation of a grayscale image

Structuring element

1	1	1
1	(1)	1
1	1	1

16	14	14	17	19	15	21
53	(57)	61	62	64	50	58
126	128	124	122	125	125	127
132	130	133	132	151	132	130
140	138	137	143	138	137	134
143	141	138	142	140	134	144
138	142	137	139	137	135	134

Input image

16	14	14	17	19	15	21
53	128	61	62	64	50	58
126	128	124	122	125	125	127
132	130	133	132	131	132	130
140	138	137	143	138	137	134
143	141	138	142	140	134	144
138	142	137	139	137	135	134

Output image
Figure 3. Block schematic of sort-3

III. ALGORITHM

Step I: First the numbers are sorted vertically *i.e.* sort elements of each column in the ascending order.

Step II: Numbers are sorted horizontally *i.e.* sort elements of each row in the ascending order.

Step III: Sort the cross diagonal elements and pick up the middle element as the median element of the window. Minimum is the first and maximum is the last element in the window of the nine elements.

The block schematic of sort-3 is shown in Figure 3.

3 x 3 window pixels values are sorted and outputs H[7:0], M[7:0], L[7:0] correspond to maximum, median and minimum values respectively.
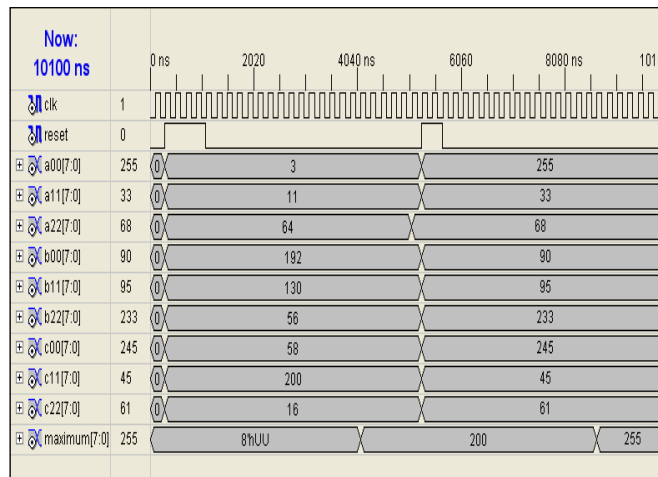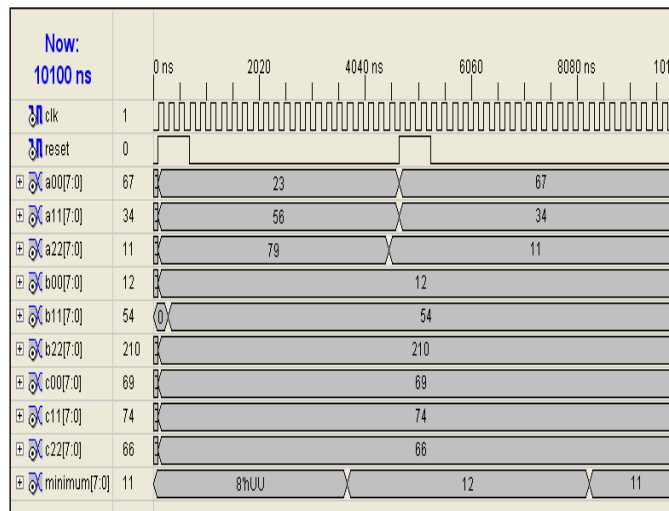

Figure 4. Simulation result of Dilation.

Figure 5. Simulation result of Erosion.

A: Implementation

The entire implementation of image acquisition, image processing and image retrieval is shown in block diagram of figure 4. In order to reduce complexity of data transactions, RAM is implemented on FPGA.
UART is implemented to felicitate data acquisition and communication between PC and FPGA board.
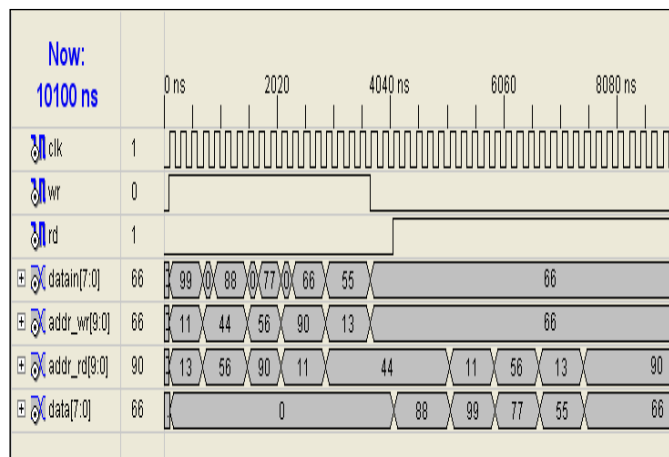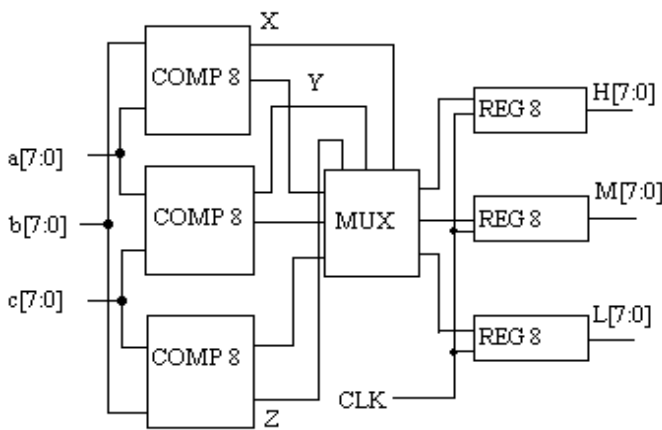

Figure 6. Simulation result of RAM

Figure 7 Block schematic of sorter

4. CONCLUSION:

In this paper, a new technique has been proposed which employs a hybrid, parallel serial input scheme that demonstrates a significant advantage over conventional input accessing methods. The design based on the above algorithm has the ability to exploit certain features.
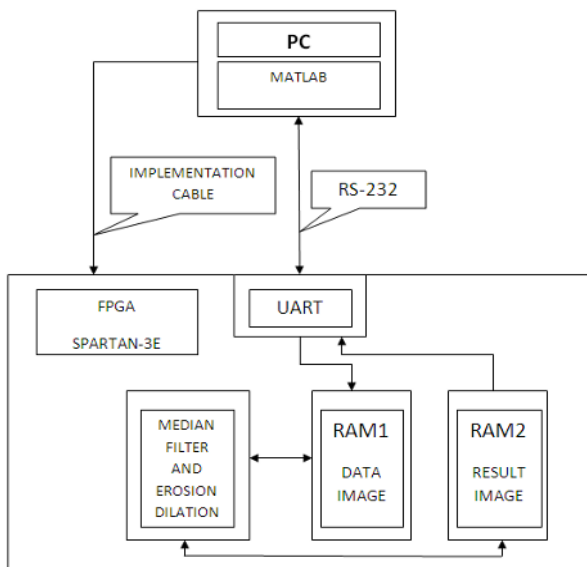

Figure 8 Block diagram of design implemented on FPGA

REFERENCES:

1. D. Baumann, J. Tinembart. Mathematical Morphology
2. Image Analysis on FPGA, IEEE Int. Conf. on Advances in Intelligent Systems Theory and Applications, 2004.
3. Daggu Venkateshwar Rao, Shruti Patil, Naveen Anne Babu, V Muthukumar , *Implementation and Evaluation of Image Processing Algorithms on Reconfigurable Architecture Using C-based Hardware Descriptive Languages*, International Journal of Theoretical and Applied Computer Sciences Volume 1 Number 1 (2006) pp. 9–34 (c) GBS Publishers and Distributors (India).
4. Soohwan Ong and Myung H. Sunwoo, *A Morphological Filter Chip Using a Modified Decoding Function,* IEEE Transactions on circuit and systems-II: Analog and digital signal processing, vol. 47, no. 9, September 2000.
5. Luca Breveglieril, Vincenzo piuri, *Digital Median Filters*, Journal of VLSI Signal Processing 31, 191–206, 2002

WEB REFERENCES:
www.xilinx.com
www.mathworks.com