

An Efficient Distributed Arithmetic Architecture for Discrete Wavelet Transform in JPEG2000 encoder

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Abstract: The JPEG 2000 image compression standard is designed for a broad range of data compression applications. The Discrete Wavelet Transformation (DWT) is central to the signal analysis and is important in JPEG 2000 and is quite susceptible to computer-induced errors. However, advancements in Field Programmable Gate Arrays (FPGAs) provide a new vital option for the efficient implementation of DSP algorithms. The main goal of project is to design multiplier less and high speed digital filters to design DWT. The convolution and lifting based approach possess hardware complexity due to multiplier and long critical paths. The Distributed arithmetic architecture is implemented to achieve multiplier less computation in DWT filtering, it is based on Look-up table approach, which may lead to a reduction of power consumption and the hardware complexity. DA is basically a bit-serial computational operation that forms an inner product of a pair of vectors in a single direct step. To speed up the process the parallel DA is implemented. In the parallel implementation, the input is applied sample by sample in a bit parallel form.

Key Words: JPEG 2000, DWT, Error Detection, DA.

1. INTRODUCTION:

In the last few years, there has been a growing trend to implement DSP functions in Field Programmable Gate Arrays (FPGAs), which offer a balanced solution in comparison with traditional devices. Digital signal processing algorithms are increasingly employed in modern wireless communications and multimedia consumer electronics, such as cellular telephones and digital cameras. Traditionally, such algorithms are implemented using programmable DSP chips for low-rate applications, or VLSI application specific integrated circuits (ASICs) for higher rates. However, advancements in Field Programmable Gate Arrays (FPGAs) provide a new vital option for the efficient implementation of DSP algorithms. FPGAs are bit-programmable computing devices which offer ample quantities of logic and register resources that can easily be adapted to support the fine-grained parallelism of many pipelined digital signal processing algorithm.

Lifting scheme, which reduces the number of computation has been proposed for the DWT. Lifting scheme has several advantages, such as in-place Computation of the wavelet coefficients, integer-to-integer wavelet transform etc. Up to now, several VLSI implementations have been proposed based on the lifting scheme. Among them, Chen proposed a multilevel lifting-based wavelet transform architecture. Chen's architecture takes only half the time for the computation of DWT when compared with other designs, but it still works under a large clock period.

Conventional lifting based architectures require fewer arithmetic operations compared to the convolution-based approach for DWT, they sometimes have long critical paths. If T_a and T_m are the delays of the adder and multiplier, respectively, then the critical path of the lifting based architecture for the (9, 7) filter is $(4 \times T_m + 8 \times T_a)$, while that of the convolution implementation is $(T_m + 2 \times T_a)$. In addition to this and for the reason to preserve proper precision, intermediate variables widths are larger in lifting -based computing. As a result, the lifting multiplier and adder delays are longer than the convolution ones. Hence convolution is a best method to reduce the delays in the computation of DWT. The efficient implementation of DWT using 9/7 filters in resource-constrained hand-held devices with capability for real-time processing of the computation-intensive multimedia applications is, a necessary challenge.

In computation of DWT the conventional multipliers adds delay to the architecture and also utilizes more hardware. Multiplier-less hardware implementation approach provides a kind of solution to this problem due to its scope for lower hardware-complexity and higher throughput of computation

2. DISTRIBUTED ARITHMETIC BASED DWT

Distributed arithmetic is a bit level rearrangement of a multiply accumulate to hide the multiplications. It is a powerful technique for reducing the size of a parallel hardware multiply accumulates that is well suited to FPGA designs. It can also be extended to other sum functions such as complex multiplies, Fourier transforms

and so on. Distributed arithmetic (DA) can be adopted to eliminate the requirement of multiplication, which may lead to the reduction of power consumption.

Most of these applications are computation intensive with multiplication and/or addition being the predominant operation. The main advantage of distributed arithmetic approach is that it speeds up the multiply process by pre-computing all the possible medium values and storing these values in a ROM. The input data can then be used to directly address the memory and the result.

A. Hardware Reduction In DA Method

The DA method reduces the hardware utilization, which increases the speed of the process, for the original equation, the hardware utilization is high.

$y = -\sum_{k=1}^k A_k(b_{k0}) + \sum_{k=1}^k \sum_{n=1}^{N-1} (b_{kn} A_k) 2^{-n} \leftarrow$ original equation hardware is reduced compare to original equation.

$y = -\sum_{k=1}^k A_k(b_{k0}) + \sum_{n=1}^{N-1} [\sum_{k=1}^{k-1} A_k b_{kn}] 2^{-n} \leftarrow$ Bit level rearrangement

B. ROM Look-Up Table Approach In DA Method

The DWT coefficients, which consist of coefficients and delays, are generated after passing through the high pass and low pass filters. For performing the filter with operation 'n' input variables, the filter coefficients are convolved with inputs. Here the coefficients are fixed. Inputs can be represented in binary. Inputs are scaled such that their absolute values will be less than 1. The inner products for various inputs can be computed and stored in advance, in ROM look-up tables. If there are n wavelet coefficients then the size of the look-up table will be 2n.

3. PARALLEL DA ARCHITECTURE

Normally Distributed arithmetic architecture is bit serial in nature, the speed of the process will be slower. To increase the speed of the process parallel distributed arithmetic architecture is implemented

In parallel implementation, we divide the input data into even samples and the odd samples based on their position. Even we can split the filter coefficients into even and odd samples. So, the even samples convolve with the even and odd filter coefficients and at the same time the odd samples also convolve with the same coefficients. So, by the same time getting the result for both even and odd samples of input. Here number of clock cycles are reduced which results in increased speed and decreased memory. Cycles the registers are loaded with the input values and then for next set of cycles the reloading operation to registers are been enabled.

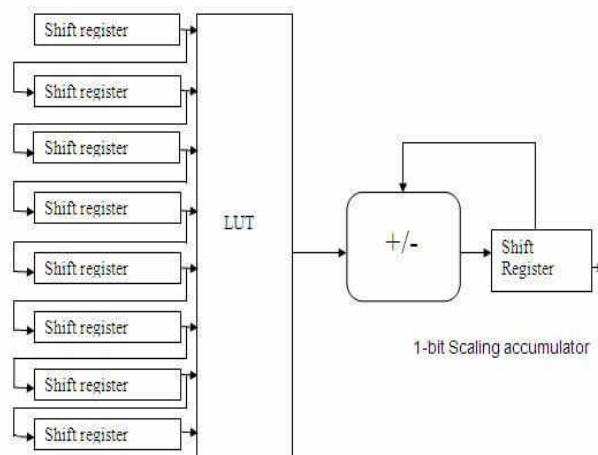


Fig3.1 PARALLEL DA ARCHITECTURE

To access the look-up table, we have the same number of registers as filter coefficients. The input $x[n]$ will enter into the serial shift register which has to access the look-up table. When the next input comes into first register, the old value will be pushed into the next register. In the same way, when next values come into registers, the old values will go off from the registers. Now, to get the address from the input values, we consider the bit positions and get the values of inputs by that bit position. For example, if we want to get the first address, we have to consider the LSBs of all serial registers. By this address we will get the first position value. In the same manner, we have to get all bit position addresses and get the corresponding values from the look-up table. While adding, we have to shift the values by the bit position value and give them to adder. Finally, we have the result, which is the convolution of the filter coefficients and the inputs.

The same architecture will be used for the both high-pass and low-pass filters. If the input is 8-bit length, then we require 8 clock cycles to get the convolved value. In computing the wavelet coefficients the filter operations are specified using floating point arithmetic. However, integer arithmetic is used in practice. Thus, the filter coefficients are truncated. This truncation reduces the accuracy of the computed coefficients.

4. LUT PARTIONING:

The LUT size in a distributed arithmetic implementation increases exponentially with the number of coefficients, the LUT access time can be a bottleneck for the speed of the whole system when the LUT size becomes large. The 4-bit LUT partitioning is optimum in terms of logic resources utilization, since this matches naturally the Virtex slice architecture, Which uses 4-input LUTs. The total size of storage is now reduced since the accumulator occupies less logic resources than the larger 8-bit LUT. Furthermore, partitioning the larger LUT into two smaller LUTs accessed in parallel reduces access time.

5. RESULTS AND DISCUSSION:

A.Simulation Result Of 1D DWT

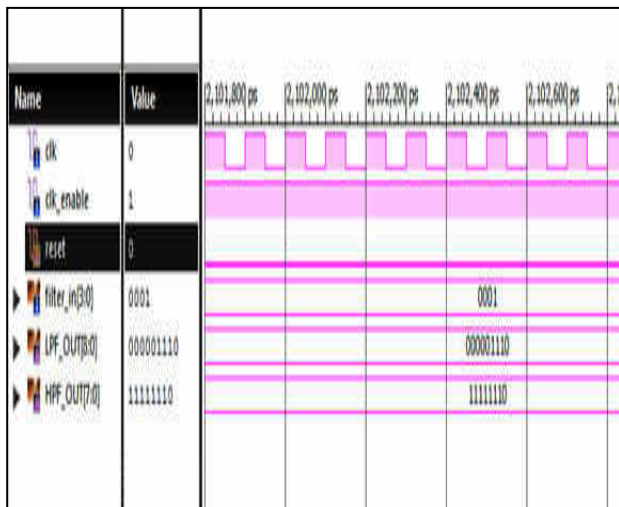
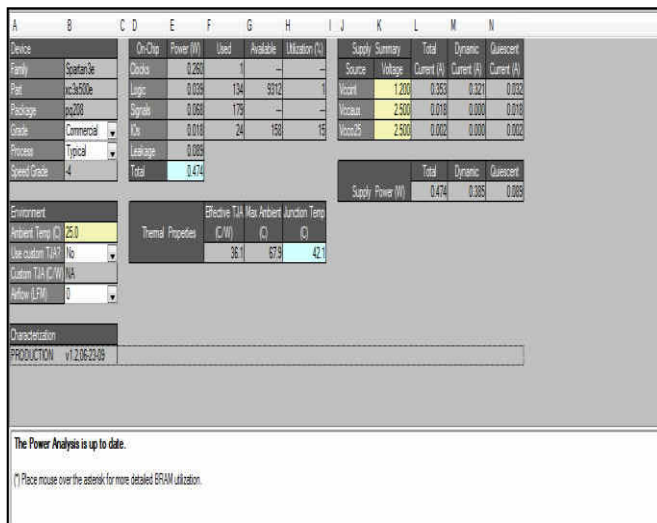


Fig 5.1 Simulation Result Of 1D DWT

B. Power Analysis Report

The power analysis has been done using Xilinx XPower analyzer, the report shows that total power consumption is 0.474w.



6. CONCLUSION AND FUTURE WORK:

In this work, the distributed arithmetic based FIR filters are designed for DWT. The main power consuming operation in DWT is filtering. In that multipliers are costlier and hence can be replaced with shifts and ROM look-up tables which are suitable for low power portable application. DA architecture is adopted for effectively performing the inner product calculations to eliminate the requirement of multiplication and increases the speed of computation, which is an efficient technique to implement on Field programmable Gate Arrays (FPGA). This method increases the speed of the computation and reduces the hardware complexity by using ROM look-up table

approach. The simulation and the synthesized results showed that the proposed method is efficient. The proposed method is suitable for various applications such as signal classification, denoising and JPEG 2000 image compression standards. In future work, when number of wavelet coefficient increases the size of the look-up table will increase, the size of the memory will be reduced by using memory reduction methodology.

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