FPGA based Design and Implementation of Decimal Matrix Code for Enhanced Memory Reliability

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Abstract: Now days, dependability of memory cells are maintained by protection codes. To avoid corruption of data and to provide security various error detection and error correction methods introduced. To avoid corruption of data most widely used codes are Error correction code (ECC) that introduces a delay penalty in accessing the information at the decoding process. Low speed performed in memory is a limitation of ECC. ECC can be contributed to the utilization of simple code such as single error correction (SEC) and Double error correction (DEC) and detection. One of the most common codes used for the memory protection is Matrix Code (MC). To improve memory reliability with lesser delay Decimal Matrix Code (DMC) is used. This code is based on structure of matrix and divide-symbol. In this paper, 32-bit Decimal Matrix Code is offered to assure the memory reliability. The design presented in this work offers DMC based error detection and correction capability up to extended errors of error bits stored in memory. Apart from this the structure area of DMC is reduced by reusing its Encoder this is called Encoder Reuse Techniques (ERT). ERT is a technique that can be used to minimize area without interrupting DMC encoder and decoder. ERT uses DMC Encoder itself to be a part of decoder. Hence the entire structure area of DMC can be reduced. Simulation and implementation are performed using Xilinx Design Tool.

Key Words: DMC, ECC, ERT, FPGA, Xilinx.

INTRODUCTION:

Now days, it's very essential to provide protection to the memory cells victimization protection codes to keep up rational level of data reliability. Various error detection and correction methods are being in a job to avoid data corruption, recollections are often protected with a slip correction code. It's given that almost all single bit errors are often detected superfluous kind of fault will upset its correct operation. This error, referred to as one event upset (SEU) or soft error. Soft error could be introduced as a bit-flip within the memory. Cell obtained of a temporary gift pulse generated by ionization. Charged particles coming reverse from sun activity and neutrons that beat the fabric will cause this ionization. Apart from one Single event upset when soft error will occur at an equivalent time during a memory array than this can be referred to as multiple bits upset (MBU) .It may end up from a high-energy element without a doubt inflicting double bit upset or an occasional incident angle distinguished several cells during a row. Unfair treatments on nucleon and heavy-ion fluxes calculate the chance of one particle agitating MBU. Against transient errors there must be a detection and correction code (EDAC) introduced that could be a recognized technique for safeguarding storage devices. Correlate example of Error detection and correction code depends on performing code is helpful for protection recollections compared to Single Event Upset owing to its effective capability to express single upsets per coded word with condensed space and performance superior than there square measure business recollections that use performing code with high-responsibility applications to extend turn out or error tolerance. So performing code isn't able to make clear in your mind the responsibility of once producing defects and MBUs from the atmosphere square measure gift. There square measure alternatives to EDAC, like (Bose-Chaudhuri- Hocquenghem) codes and RS (Reed-Solomon), supported finite-field (also called mathematician field) arithmetic, which may address multiple faults. In this thesis, 32-bits Decimal Matrix Code was planned to declare the reliability of memory. Decimal matrix code (DMC) beginning on divide-symbol is obtain able to boost memory reliability with the employment of lower delay the planned DMC uses decimal whole number subtraction and decimal whole number addition is employed to get the capacity of error detection ability. ERT technique is employed to reduce the space of DMC while not disturbing the total encryption and secret writing processes. Decimal Matrix Code is a technique employ in a encoder and this one is to be a part of the decoder. Consequently, the entire circuit space of Decimal Matrix Code is reduces of encoder part. Next A Verilog Description has been adopted to embed the low power design.

Transient multiple cell upsets (MCUs) are getting considerable issue within the reliability of memories visible to emission surroundings. To avoid MCUs from moving data corruption, extra comprehensive error correction codes (ECCs) square

measure sometimes adapted for safeguard memory though the most disadvantages it need larger delay overhead. Lately new matrix codes (MCs) recognized to avoid such conditions. Decimal matrix code (DMC) based on divide-symbol is available to extend memory reliability with lower delay. The planned Decimal Matrix Code uses decimal law to achieve error detection capability. The encoder-reuse technique (ERT) is obtainable to decrease the space of decoder by using encoder as a part of decoder. Whereas not disturbing the entire cryptography and decryption ways. Encoder employ Technique uses DMC encoder himself to be portion of the DMC decoder. To avoid the data corruption causes due to Multiple Cell Upsets more challenging error correction codes (ECCs) are generally used to protect memory. The challenge here are double error correction codes and the error correction proficiencies are not superior. To conquer these defects a new method is introduced that explained below. In this paper, Decimal Matrix Code (DMC) offered divide-symbol to improve memory reliability with lower delay. The offered DMC uses decimal algorithm uses decimal number subtraction and decimal number addition to obtain the maximum error detection capability and to reduce the area without upsetting the complete encoding and decoding processes encoder-reuse technique (ERT) is offered.

LITERATURE REVIEW:

Decimal matrix code is one of the error detection and correction method used to correct errors up to some place in reference [1, 4, 7, 8, 13, 17, 20] DMC encoder and ERT decoder is proposed to reduce the error capability and to reduce the area of decoder. This can be achieve by using Verilog HDL and synthesized using Xilinx integrated software environment the design simulated using ISIM Simulator. The design implementation is done on Xilinx Spartan 6 xc6slx45-cgs324-3. Reference [2], represents a review on FPGA based DMC algorithm given by number of scholars work and compare the different work. In Reference [3], protection code utilized decimal algorithm to detect errors apart from error detection maintenance of reliability has achieved by changing Carry Save Adder (CSA). The proposed method also combined with traditional 2-D repair approaches such that row and column failures and defects on multiple bits are repaired, and isolated defects are handled by the SEC-DED codes. Reference [5, 12] represents a novel Parity Matrix Code (PMC) based method. A parity algorithm (matrix addition and matrix multiplication) is used to identify and fix many errors which need less number of redundant bits compared to decimal matrix codes (DMC). This fixes maximum number of slips in memories and has least performance overheads. In reference [6] a new application of Boom Filters has been proposed. BFs use an efficient error correction code to prevent the data inside the memory .MSB to LSB parallel prefix comparator is used inside the bloom filter to speed up the comparison by reducing the switching activity of the comparator structure. In this paper DMC was used to assure the reliability of memory and protect the memory by performing error detection and correction.

In reference [9, 16] modified-DMC was proposed to protect memories from radiation induced errors. Hamming encoder and decimal algorithm is combine who allows detection and correction of large MCUs. And ERT technique is use to reduce the area overhead of extra circuits. In reference [10, 11, 12] novel per-code DMC was proposed to assure the reliability of memory. The reliability of system is achieved by detecting and correcting more errors and this can be achieved by using decimal algorithm. Moreover, the proposed decimal error detection technique is an attractive outlook to detect MCUs in CAM because it can be combined with BICS to give an enough level of immunity. For the MC [14] based on Hamming, when two errors are detected by Hamming the vertical syndrome bits are activated so that these two errors can be corrected. As a result MC is capable of correcting only two errors in all cases. Reference [15] deals with two error correcting codes Decimal Matrix Code (DMC) and Parity Matrix Code (PMC) The DMC utilized decimal algorithm to obtain the maximum error detection capability and PMC utilized hamming algorithm to detect errors, so that more errors can be detected and corrected. And both techniques use Encoder-Reuse Technique (ERT) to minimize the area overhead. In reference [18] novel Decimal Matrix Code (DMC) based on divide- symbol is proposed to enhance memory reliability with lower delay overhead. ERT used to reduce the area overhead of extra circuits in this paper Meta-Cure is proposed which exploits built-in ECC and replication in order to protect pages containing critical data. In reference [19] Parity based matrix codes is proposed to increase the error handling capability. Proposed method will increase the data accuracy of the memory.

DMC Encoder and Decoder Design Implementation Methodology:

Enhanced memory dependability is offered by Different Decimal Matrix Code (DMC) designed using matrix based arrangement of data. In this proposed method to identify the errors Decimal algorithm use decimal addition. Error detection capability is increased Using Decimal algorithm thus the reliability of memory is improved. In this paper, Decimal Matrix Code is presented to declare dependability of the memory in the existence of Multiple Cells Upset's with reduced routine overheads. In the Encoder the information bits D are applied to the encoder, and obtain vertical redundant bits V and the Horizontal redundant bits H as the output and this output is coded with redundancy bits and stored in memory. In case Multiple Cells Upsets occur in the memory, these faults can be modified in the decoding process. Encoder reuse can be

performed at the decoding process, decimal algorithm using ERT technique which becomes the advantage in terms of reduce g the area. We can minimize the area without disturbing the encoder and decoder circuit in the fault-tolerant memory. In the proposed work, 32-bit data division method is used to implement the DMC encoder and then encrypt the data to generate redundant bits. In divide method the N-bit data is divided into K-symbols of m-bit size, thus, N = K x m, and then the K symbols are arranged in a 2-D matrix of size k1 x k2, where k1 and k2 represents the number of row and column respectively. To the selected symbol per row decimal integer addition is perform to generate the horizontal redundancy bits this is the reason to identify each m-bit symbol. Decimal addition is performing by considering each symbol as a decimal integer. Parity generation operation is perform among the bits of the column to obtain the vertical redundancy bits. The proposed DMC does not need to change the physical structure of the memory as the steps are implemented in logical form. During the encoding process the 32-bits of data, D32…D0 are considered into symbols of 4-bit and arranged in a matrix of 2 rows x 4 column. Thus, N = 32, K = 8, m = 4, k1 = 2, and k2 = 4. The equations that are implemented to obtain the horizontal and vertical redundant bits are shown as follows:

Equations for generating horizontal bits

$H_4H_3H_2H_1H_0 = D_{11}D_{10}D_9D_8 + D_3D_2D_1D_0$

$H_9H_8H_7H_6H_5 = D_{15}D_{14}D_{13}D_{12} + D_7D_6D_5D_4$

$H_{14}H_{13}H_{12}H_{11}H_{10} = D_{27}D_{26}D_{25}D_{24} + D_{19}D_{18}D_{17}D_{16}$

$H_{19}H_{18}H_{17}H_{16}H_{15} = D_{31}D_{30}D_{29}D_{28} + D_{23}D_{22}D_{21}D_{20}$

Equations for generating vertical bits

V0 = D0 Xor D16
V1 = D1 Xor D17
V2 = D2 Xor D18
V13 = D13 Xor D29
V14 = D14 Xor D30
V15 = D15 Xor D31

The encoder generates the horizontal redundant bit H and the vertical redundant bit V. The proposed architecture of fault-tolerant memory is show in Figure 3.1.

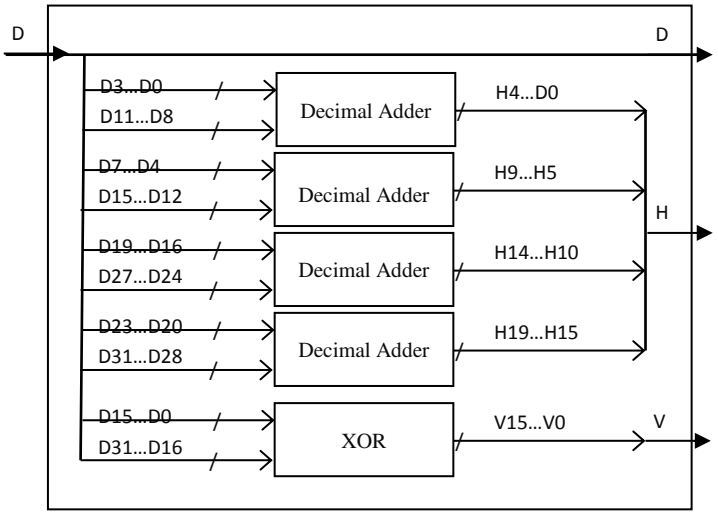

Figure 3.1 32-bit Architecture of DMC Encoder

The DMC encoded codeword consist of D, H and V. This code work is then stored in the memory. This arrangement of data and the redundant bit generation is described with the help of example as follows:

32-bit Data arranged in matrix

0	1	0	1	0	1	1	0	0	1	1	0	1	0	1	0
1	1	0	0	1	0	1	0	0	0	1	1	0	1	0	1

2-bit Data arranged in symbol matrix (2 x 4)

Symbol-3	Symbol-2	Symbol-1	Symbol-0
0101	0110	0110	1010
1100	1010	0011	0101
Symbol-7	Symbol-6	Symbol-5	Symbol-4

Generated Horizontal Redundancy Data:

Symbol-0 + Symbol-2 = 10000
Symbol-1 + Symbol-3 = 01011
Symbol-4 + Symbol-6 = 01111
Symbol-5 + Symbol-7 = 01111

Generated Vertical Redundancy Data:

1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	1

If MCUs are introduced in the memory then the decoder can correct the errors. In the decoder the redundant bits are again generated from the data bits that were stored in memory. If the memory data is represented by D' then H' and V' represents the redundant bits generated by the decoder. In the decoding process, the stored redundant bits (H and V) and the generated redundant bits (H' and V') are used to generate the syndrome bits. These syndrome bits are further used to locate the position of error in the data that is fetched from memory and also to correct the error-bits. The architecture of the proposed decoder is shown in Figure 3.2.

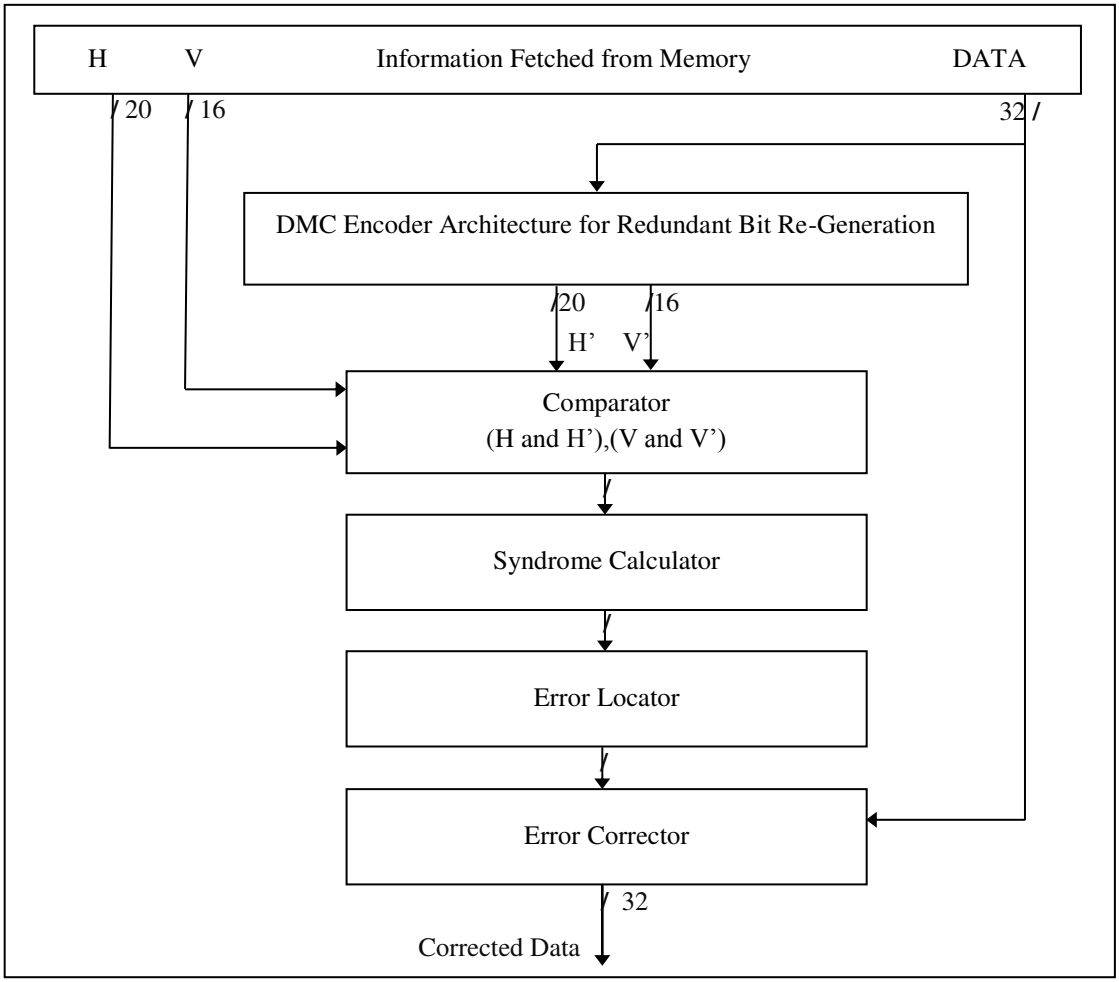

Figure 3.2 Proposed Architecture of Fault tolerant Memory using Decimal Matrix Decoder

In the proposed work the syndrome is generated by logical comparator using XOR gate. The conventional design of error syndrome generator logic utilizes decimal subtractor logic to generate the syndrome data. Figure 3.3 Syndrome generation using proposed XOR-comparator (a) Vertical Syndrome, (b) Horizontal Syndrome. The equations that are implemented to obtain the horizontal and vertical syndrome bits are as follows:

$$V_{syn} = V \text{ xor } V'$$
$$H_{syn} = H \text{ xor } H'$$

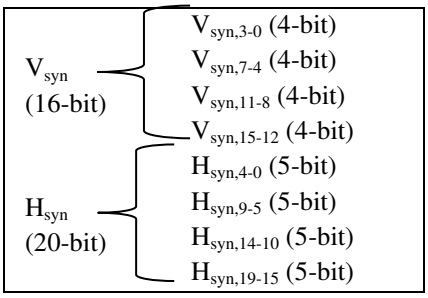

Figure 3.3 Grouping of Syndrome Bit

The non-Zero presence of any bit or bits of Hsys or Vsys, indicates the presence of the error in the stored data. To find the symbol that contains error the horizontal and vertical syndrome bits are grouped with the same length as that of horizontal and vertical redundant bits. This grouping is depicted in Figure 3.4.

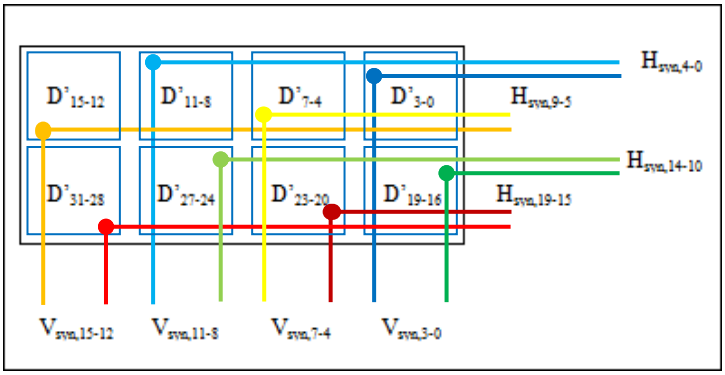

Figure 3.4 Error Location using Syndrome Data

SYNTHESIS AND IMPLEMENTATION RESULTS:

FPGAs have acknowledged being very effective and efficient procedures to work on DMC. They can perform a much closer data-rate and to offer enhanced safety than related software executions. The Field Programmable Gate Array (FPGA) is a controlling tool to identify the functionality to the design. Xilinx ISE (Integrated Software Environment) is a software device which produced by synthesis and analysis of HDL designs, it can perform timing analysis which can be perform enabling the developer to synthesize designs, to inspect RTL diagrams, simulate a proposal's reaction to altered stimuli, and configure the target device with the programmer. The different modules are designed using VHDL simulated using ISIM simulator.

Figure 4.1 (a)

Figure 4.1 (b)

Figure 4.1 (a) Arrangement of Hardware Setup kit (b) Reset Mode Operation Display on LCD.

The hardware based design simulation is performed on various input values. An example with input hexadecimal values of

both Encoder and decoder with data=F5AFF6AC, hrb=CD332 and vrb=0303 is shown in Figure 4.2 (a) and Decoder with no error with Figure 4.2 (b) respectively.

Figure 4.2 (a)

Figure 4.2 (b)

Figure 4.2 (a) Encoder Input mode display (b) Decoder output without error

CONCLUSION:

The capability of error detection and correction can be obtained by Decimal Matrix Code Algorithm. Matrix Code is us used to maintain the reliability of memory. Data reliability is enhanced by using decimal algorithm that provides protection to code word by detecting errors. The results in this work show that this scheme has a better-quality protection level against large MCUs in memory. In this paper, a successful design of DMC encoder and decoder with 32-bit data is performed by implementing the design on Xilinx FPGA device. The different Modules are designed using VHDL and synthesized using Xilinx Integrated Simulation Environment (ISE) Tool. The simulation of designs is performed using ISIM Tool. There is always a scope of improvement in all the existing designs. The present work can also be improved in future by reducing the number of redundant bits. Another scope of future work in reference to present work leads to an increase in the error detection efficiency of the code by introducing some modifications.

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