Design and Implementation of Efficient Reed Solomon code with Low Delay Single Symbol Error Correction

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Abstract: This paper presents a compact and fast field programmable gate array and we know that efficiency is one of the important parameter in order to achieve high performance in mobile communication environment using modulation and coding technique. Where as in mobile communication application higher capacity and data rate is the basic requirement for reliable communication. To avoid the data corruption, error correction codes are widely used to protect memories and also storage devices and to improve the communication system but previously there is usages of ECC but this introduce a delay penalty in accessing the data as encoding or decoding as to be performed and major issue is that conventional ECC introduces more delay during error computation so the main challenge is that those codes should minimize the delay and area penality.so here the best multiple error correcting code used is reed Solomon code. In this single symbols error correction codes based on reed Solomon codes that can be implemented with low delay are proposed and evaluated.

Key Words: Error correction codes, reed-Solomon codes, DRAM memory module, soft errors, Galois field, FPGA Module, Error Decoder

1. INTRODUCTION:

Digital communication system is used to transport an information bearing signal from the source to a user destination via a communication channel. A code is the set of all the encoded words, the code word that an encoder can produce. When actual set of data encoded it becomes a code. Data corruption caused by errors is a significant issue in memories and channels. Errors can be caused for example by radiation induced soft errors that affect one or more memory cells and change their values. Other types of failures cause permanent damage such that the device no longer provides correct data. To ensure that data is not corrupted when failures occur, error correction codes (ECCs) are widely used in memories [1]. ECCs adds some additional parity check bits to each memory word such that errors can be detected and corrected. In the proposed system it describes mainly data corruption in noisy Channel .Parity additional bits reduces the effective capacity of the memory. Other overheads introduced by the ECC are the encoding and decoding circuitry. This circuitry has an impact also on the delay as the data has to be encoded when transmitting over a channel and decoded when reading from it. In many cases, the decoding is more complex because its having several steps than the encoding and limits the speed of the ECC [1].Traditionally single error correction double error detection(SEC-DED) codes are used to protect memories [3].But in the proposed system Multiple byte of error in the data signal is detected and corrected. in view point of performance as well Delay .This is very attractive for memory modules and channel as and when the number of bits in the devices matches those of the symbols in the RS code, failures in one device can be corrected. In fact, for this reason RS codes are commonly used to protect main the polynomial corresponding to a code word is a multiple of a specific polynomial, called generator polynomial g(x). Reed-Solomon error correcting codes (RS codes) are widely used in communication systems and data storages to recover data from possible errors that occur during transmission and from disc error respectively. There two types of Errors, whenever bits flow from one point to another, they are subject to unpredictable changes because of interference. This interference can change the shape of the signal. In a single-bit error, a 0 is changed to a 1 or a 1 to a 0. The term single-bit error means that only 1 bit of a given data unit (such as a byte, character, or packet) is changed from 1to 0 or from 0 to 1.The term burst error means that 2 or more bits in the data unit have changed from 1 to 0 or from 0 to 1.Reed Solomon code is a linear cyclic systematic non-binary block code. In the encoder Redundant symbols are generated using a generator polynomial and appended to the message symbols. In decoder error location and magnitude are calculated using the same generator polynomial. Then the correction is applied on the received code. Reed-Solomon coding is a type of forward-error correction that is used in data transmission (vulnerable to channel noise) plus data-storage and retrieval systems.

2. LITERATURE SURVEY:

Channel coding is an important signal processing operation for the efficient transmission of digital information over the channel. In channel coding the number of symbols in the source encoded message is increased in a controlled manner in order to facilitate two basic objectives at the receiver one is Error detection and other is error correction. Error detection and error correction to achieve good communication is also employed in devices. It is used to reduce the level of noise and interferences in electronic medium. The amount of error detection and correction required and its effectiveness depends on the signal to noise ratio (SNR) [1]. A channel code is a broadly used term mostly referring to the forward error correction code. Forward error correction (FEC) is a system of error control for data transmission, whereby the sender adds redundant data to its messages, also known as an error correction code. This allows the receiver to detect and correct errors without the need to ask the sender for additional data. FEC is applied where retransmissions are relatively costly or impossible. FEC information is usually added to most mass storage devices to protect against damage to the stored data [2]. There are many types of block codes, but the most notable is Reed Solomon coding, Golay, BCH, Multidimensional parity, and Hamming codes are other example of block codes.

Reed Solomon is an error-correcting coding system that was devised to address the issue of correcting multiple errors – especially burst-type errors in mass storage devices (hard disk drives, DVD, barcode tags), wireless and mobile communications units, satellite links, digital TV, digital video broadcasting (DVB), and modem technologies like xDSL [3]. Reed-Solomon codes are an important subset of non-binary cyclic error correcting code and are the most widely used codes in practice. These codes are used in wide range of applications in digital communications and data storage. Reed Solomon describes a systematic way of building codes that could detect and correct multiple random symbol errors. By adding t check symbols to the data, an RS code can detect any combination of up to t erroneous symbols, or correct up to $\lfloor t/2 \rfloor$ symbols. Furthermore, RS codes are suitable as multiple-burst bit-error correcting codes, since a sequence of b + 1 consecutive bit errors can affect at most two symbols of size b. The choice of t is up to the designer of the code, and may be selected within wide limits.

Rapid growth in internet and mobile technology, exchange of information is common practice. Information may be text, audio, video etc. form. Transmission of information through a physical medium or wireless medium, possibility that data get corrupted this leads to an error in a random only selected locations of a symbol or the entire symbol. To have a reliable communication through a communication channel that has an acceptable Bit Error Rate(BER) and High Signal to Noise Ratio(SNR) error correcting codes are used .These codes are used to detect and correct a specific number of error which may occur during transmission of message over a communication channel. There are different types of Error correction codes are used in present digital communication system based on the type of channel noise. few of them are Hamming code ,Low Density Parity check code (LDPC),Bose Chaudhuri Hocquenghem code (BCH),Reed Solomon Code (RSC),and Turbo Code(TC).These codes are different from each other in their complexity and implementation .BCH codes are widely used in the area like ,mobile communication, Digital communication, Satellite communication ,Optical and Magnetic storage system and Computer Network etc. In this work (15, 7) BCH encoder and decoder is implemented on Spartan 3E FPGA. For designing the BCH codes, two coding techniques are used .They are systematic codes and Non-systematic codes. In case of systematic codes original message d(x) is as it is in the encoded word c(x).where as in case of non –systematic code encoded word c(x) is obtained by multiplying message d(x) with generator polynomial G(x). At the transmitter side using encoder circuits binary digits are encoded by appending some extra bits with message bits also known as parity bits. The parity bits and message bits together called as ‘code word’. If error presents in received data within a correction limits, the error will be corrected and original message is retrieved.

Digital filters are widely used in signal processing and communication systems. In some cases, the reliability of those systems is critical, and fault tolerant filter implementations are needed. Over the years, many techniques that exploit the filters’ structure and properties to achieve fault tolerance have been proposed. As technology scales, it enables more complex systems that incorporate many filters. In those complex systems, it is common that some of the filters operate in parallel, for example, by applying the same filter to different input signals. Recently, a simple technique that exploits the presence of parallel filters to achieve fault tolerance has been presented. In this brief, that idea is generalized to show that parallel filters can be protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC. This new scheme allows more efficient protection when the number of parallel filters is large. The technique is evaluated using a case study of parallel finite impulse response filters showing the effectiveness in terms of protection and implementation cost. FPGA-based designs are more susceptible to single-event upsets (SEUs) compared to ASIC designs, since SEUs in configuration bits of FPGAs result in permanent errors in the mapped design. Moreover, the number of sensitive configuration bits is two orders of magnitude more than user bits in typical FPGA-based circuits. A

high-reliable low cost mitigation technique which can significantly improve the availability of designs mapped into FPGAs. Experimental results show that, using this technique, the availability of an FPGA mapped design can be increases to more than 99%. A low-cost and high reliable soft error mitigation technique based on check pointing. A very small auxiliary FPGA is utilized to store checkpoints, compare the checksums, and reconfigure the main FPGA. Experimental as well as analytical results show that the availability of a protected design based on this technique increases to more than 99.6%.

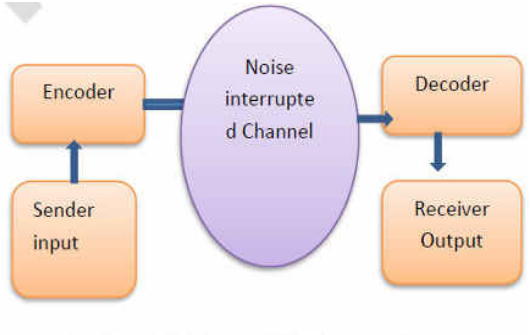

Figure 1: Basic Block diagram of digital data transmission system

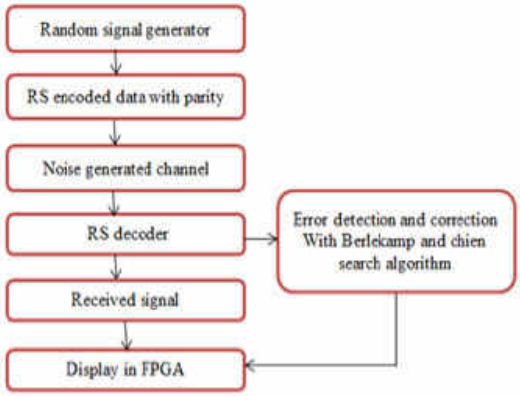

Figure 2: simple flow diagram of proposed system

3. CODES:

A. Reed Solomon code

Reed-Solomon codes are block-based error correcting codes with a wide range of applications in digital communications and storage. Reed-Solomon codes are used to correct errors in many systems. Reed-Solomon error correction has several applications in broadcasting and memories etc. Hardware implementations of encoders and decoders for Reed-Solomon error correction are complicated and require some knowledge of the theory of Galois fields on which they are based. The Reed-Solomon decoder processes each block and attempts to correct errors and recover the original data. The number and type of errors that can be corrected depends on the characteristics of the Reed-Solomon code. Proposed system computed for code size (255,223) it's in the form of (n,k) where n-k=2t,there is 32 parity bytes up to 16 byte of data error can be corrected.

B. Galois fields

In order to understand the encoding & decoding principles of Reed Solomon code, one should thorough knowledge of finite fields known as Galois fields. For any prime number p there exists a Galois field GF (p) which contains exactly p elements. It is quite possible to extend GF (p) to an extension of pm elements making it GF (pm) where m is a non-zero positive integer. A Galois also called finite field it has the property that arithmetic operations (+,-,x,/ etc.) on field elements always have a result in the field. A Reed-Solomon encoder or decoder needs to carry out these arithmetic operations. These operations require special hardware or software functions to implement.

C. RS Encoder

Encoder side is simple where data to be send is encoded with parity bit in the proposed system 32 byte of parity is added at the end of data. To encode the message, the message polynomial is first multiplied by *xn-k* and the result

divided by the generator polynomial, $g(x)$. Division by $g(x)$ produces a quotient $q(x)$ and a remainder $r(x)$ where $r(x)$ is of degree up to n-k-1.

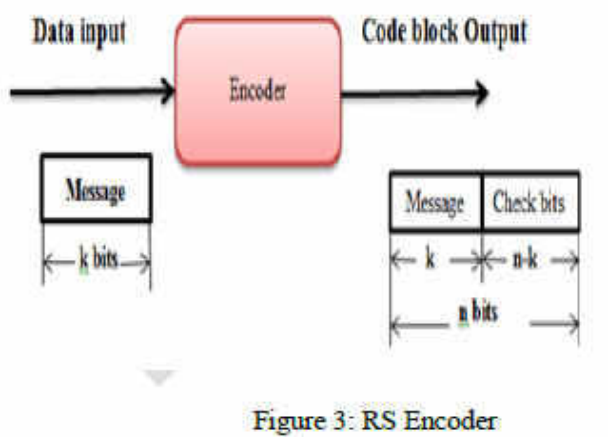

Figure 3: RS Encoder

D. RS Decoder

As soon as data received from channel which given to RS decoder which first checks whether received code word is correct or not if it is incorrect then first error detection is done and once error detected means it tell location and error magnitude that calculated with several algorithm like berlekamp messey and chien search algorithm its explained with block diagram shown in figure [14].

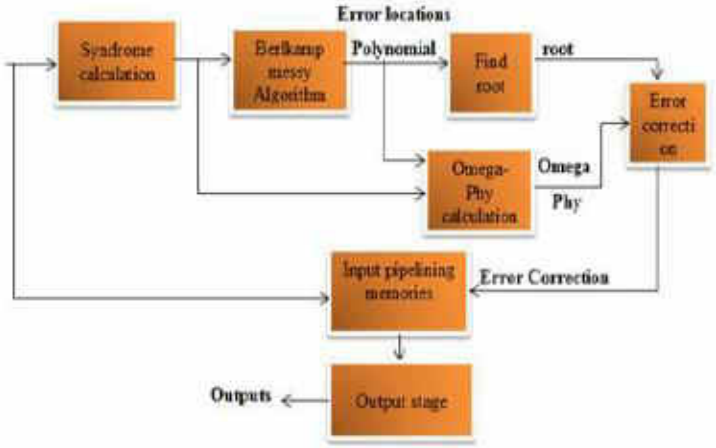

Figure 4: Block diagram of RS decoder

4. SIMULATION RESULTS:

Encoding of data is done where parity bits get added and transmitted over a channel (in the proposed system up to 224 byte the data and remaining 32 bytes are parity bits total 255 code word). Here error is get added to encoded data (to show this forcibly noise is xor with input data)so data is received at channel is corrupted shown in second simulation figure so in order to correct these error data is given to RS decoder by using algorithm data is obtained across decoder is error free shown in figure.

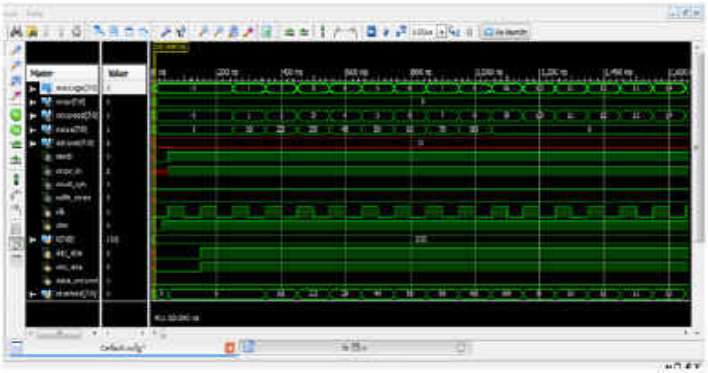

Figure 5: Encoder output and noise get added to data when transmitted over a channel

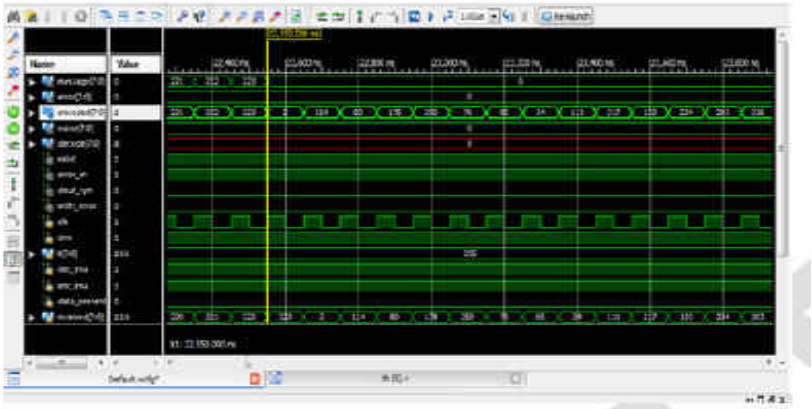

Figure 6: Simulation shows parity bits (each symbol having 8 bits)

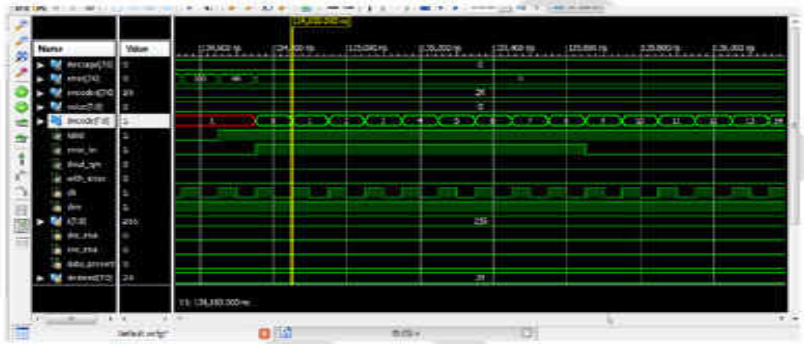

Figure 7: Decoder output

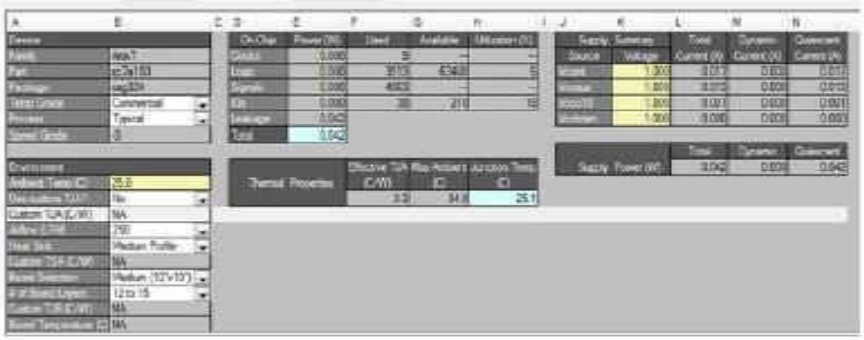

Figure 8: power analysis

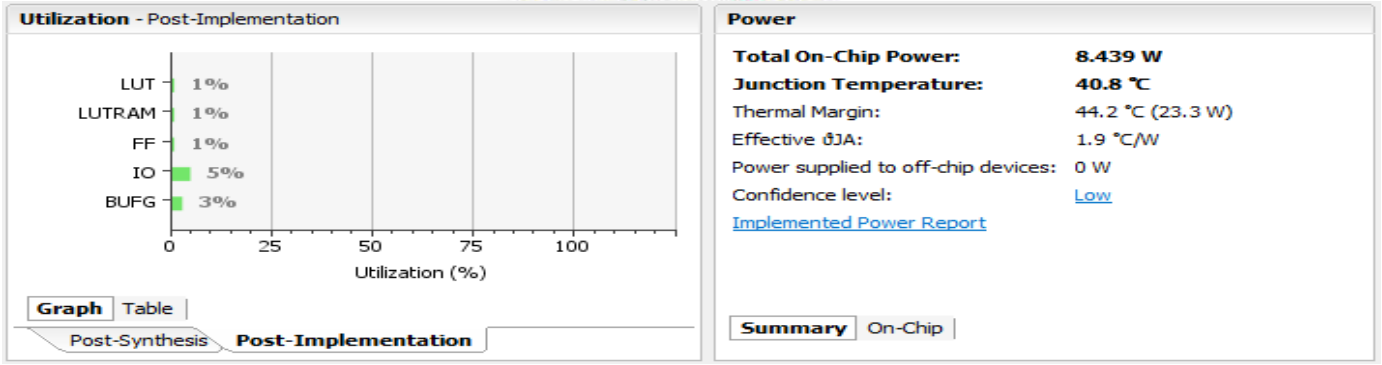

Figure 9: Area and power report

CONCLUSIONS:

In this paper, new codes based on modifications of single error correction Reed Solomon (SEC RS) codes have been proposed with the objective of reducing delay. The codes have been implemented and evaluated. The examples used for evaluation correspond to real configurations commonly used in memory modules. For those, the proposed codes enable significant delay reductions in encoding and decoding delay. This makes the modified codes attractive for high-speed memories. Future work will consider the evaluation of the proposed codes to protect other types of memory like for examples caches. When a RS Decoder corrects a symbol, it replaces the incorrect symbol with the correct one, whether the error was caused by one bit being corrupted or all of the bits

being corrupted. Thus, if a symbol is wrong, it might as well be wrong in all of its bit positions. This gives RS codes tremendous burst-noise advantages over binary codes [7]. Here Error detection and correction techniques have been used which are essential for reliable communication over a noisy channel. A compact and fast hardware implementation technique of Reed Solomon Encoding and Decoding algorithm were presented. The design was implemented in real hardware with Spartan 6 FPGA. The results demonstrate that the Reed Solomon codes are very efficient for the detection and correction of burst errors. As mentioned above, RS codes are based on the finite fields so they can be extended or shortened. Reed Solomon codes provide a wide range of code values that can be chosen to optimize performance. RS codes are used significantly in Wireless Communication (mobile phones, microwave links), Deep Space and Satellite Communications Networks (CCSDS), mass storage devices (hard disk drives, DVD, barcodes), digital TV, digital video broadcasting (DVB), and Broadband Modems (ADSL,VDSL, SDSL, HDSL etc.). Technologies are becoming smarter and compact day by day, so we hope our work will add new dimension in that trend.

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