A Review on various DSRC application of FM0/Manchester encoder-decoder based on VLSI

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Abstract: *The process of communication mainly depends on encoding and decoding of data transmission. The secure transmission of data is very important in communication system. For the secured data transmission there are different types of techniques are used for encoding and decoding of data. The different architectures use different forms of encoding-decoding techniques such as Miller, NRZ, FM0 and Manchester encoding which provide the security. These type of technique use according to their needs and have their own importance. This type of technique generally used finite state machine (FSM) for encoding to provide the corresponding output. These techniques are very strong; it provides the result without losing their parameters. As a result the speed increased. The purpose of FM0, Manchester encoding and miller is to balance the DC output, it also enhance the signal reliability.*

Key Words: *Miller encoder, DSRC, FM0 encoder, VLSI, Manchester encoder, SOLS technique*

1. INTRODUCTION:

Various Types of Encoding and decoding are used in data communications. For the transportation system dedicated short-range communication (DSRC) techniques are used. The transportation system generally based on or two ways medium range communication techniques. There are two types of categories are used in DSRC application such as vehicle-to-roadside and vehicle to vehicle. Generally DSRC (dedicated short-range communication) is allowing collision prevention applications. By using these types of application it exchange the data at very high speed between the vehicles and the roadside vehicles. These applications are very frequent for the data transmission based on the DSRC application.

Based on DSRC application the DOT (Department of U.S. transportation) finish the V2V (vehicle-to-vehicle) communication. US can address up to 82% of all collapse, saving potentially thousands of lives unimpaired drivers, and billions of dollars. The plan of U.S. by NHTSA (National Highway Traffic Safety Administration) is going to decide in 2013 requires to develop the DSRC application. It develops the new techniques to encourage the dedicated short-range communication (DSRC) for the development of the new vehicles in U.S.

The DSRC activate the sending and broadcasting among the vehicle for the issues of safety in the V2V, and for the public information announcement. The safety comprise of blind-spots, collision-alarms, inter-car distance etc. The focus of intelligent transportations services by the vehicle-to-roadside, such as ETC (Electronic toll collection) system. The ETC collecting the toll automatically or electrically this is accomplished by the contactless IC-card platforms. Additionally, the ETC has different applications such as payment for gas-refuelling and parking-services. Therefore, the dedicated short-range communication (DSRC) plays an important role in the automobile industry. Different countries implemented the standard of dedicated short-range communication (DSRC) by the several organizations. These (DSRC) dedicated short-range communication standards are shown in Table I.

TABLE I

	AMERICA	JAPAN	EUROPE
ORGANIZATION	ASTM	ARIB	CEN
CARRIER FREQUENCY	5.9GHz	5.8GHz	5.8GHz
DATA RATE	27 Mbps	4 Mbps	500kbps
MODULATION	OFDM	ASK	ASK/PSK
ENCODING (DOWNLINK)	Manchester	Manchester	FM0

Independently the goals of data rates are at 500 Kbps, 27 Mbps and 27 Kbps at the carrier frequencies rates of 5.8 and 5.9 GHz. It consists of different methods of modulations such as PSK, ASK, and OFDM. Usually, transmitted signal waveforms are probable to be mean of zero for the strength noise. It also referred to balance the DC output, because the transmitted signals are of subjected in a binary sequence of 0 or 1. It is difficult to obtain the dc-balance in this

sequence. To avoiding these types of difficulties the different techniques are presented in this paper can provide the transmit signal with dc- balance outputs. For downlink it is widely used for both FM0 and Manchester codes for designated.

Both FM0 and Manchester codes provides encoding techniques for the suitable transmission of data information so that it can convert the data information into a suitable form for the transmission. Both the techniques are used for the security purpose. Generally, there are different type of encoding techniques are used for the serial data communication. The different types of methods such as FM0, Manchester encoding, Miller encoding, NRZ, FM1, RZ, etc. are used for encoding the secure data for transmission. These types of techniques are used at transistor levels. Generally it is also used for optical communication, for minimizing the critical area, for path- delay, and buffer size by adding a minimum number of buffers in that. Baseband processors consist of a PIE reader, UHF RFID Reader, FM0 decoder, or Miller decoder, for achieving the higher efficiency and accuracy for encoding and decoding purpose. There is a need of having a high frequency clock. The architecture system of DSRC transceiver is as shown in Fig 1.

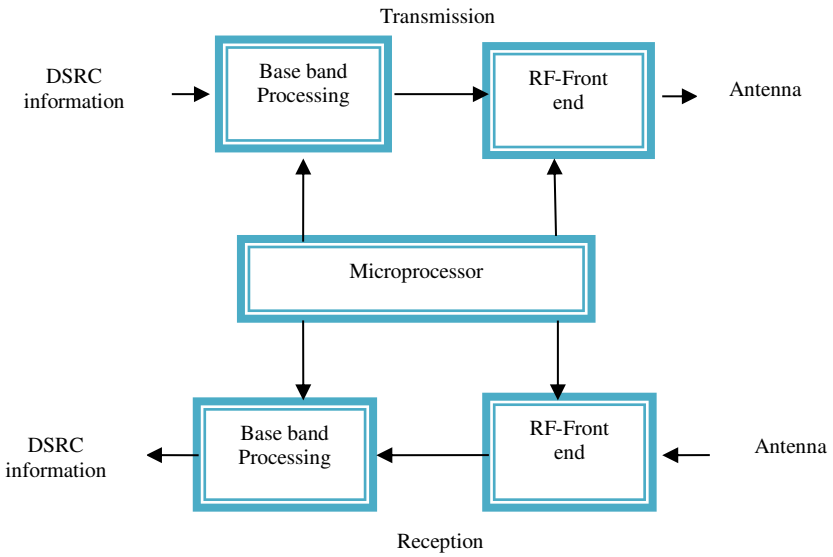

Fig. 1 DSRC Transceiver

2. REVIEW WORK:

In Reference [1, 9] work proposed the architecture by using SOLS techniques by using the fully reused Very Large Scale Integration technique for both the FM0 and Manchester encoding. The drawbacks of hardware utilization reduce by using the SOLS techniques. The two core techniques are used (1) Area compact retiming and (2) balance logic-operation sharing technique. The techniques of Area-compact retiming are used to reduce the problem of hardware similar to numbers of transistor. The other techniques of balance logic operations are used to share the help for identifying the logic components which may capably combine both the FM0 and Manchester encoding techniques. This paper proposed to work on some parameter as power consumption, operating at maximum frequency and TSMC etc.

In [2, 4, 13, 18] proposed the work on architecture by using the SOLS techniques by fully reused VLSI technique for both the FM0 and Manchester encoding techniques. The hardware utilization eliminates the limit by the SOLS techniques. . The two core techniques are used (1) Area compact retiming and (2) balance logic-operation sharing technique. The techniques of Area-compact retiming are used to reduce the problem of hardware similar to numbers of transistor. The other techniques of balance logic operations are used to share the help for identifying the logic components which may capably combine both the FM0 and Manchester encoding techniques. By using the SOLS techniques the enhancement hardware rate is 57.14% to 100% for both the techniques of FM0 and Manchester encoding. The Taiwan Semiconductor developed Company (TSMC) 0.18-µm 1P6M CMOS technologies post the layout techniques simulation for the presentation of this paper. The Manchester and FM0 encodings may have highest frequency of 2 GHz and 900 MHz respectively. For the Manchester encoding the power consumption is 1.58 mW at 2 GHz and for the FM0 encoding 1.14 mW at 900 MHz. The circuit core area is 65.98×30.43 µm2. This paper present the architecture developed the fully reused VLSI.

In [3] author proposed the work on input system, it unbalance the calculation of time result by the problem of the MUX−1. It begins the logic-faults on coding techniques. By using the XNOR gate with inverter rather than the XOR gates it will overcome the problem of this paper and this becomes the MUX-1 inputs and it balance the time of computation. The coding for the implementation of FM0 and Manchester encoding will depends on the Mode and CLR signals. The designing of both the mode of FM0 or Manchester independently allocated to the system controllers. When the code for both the FM0 and Manchester is adopted, all logic components proposed VLSI architecture were utilized and it will provide the better result for the hardware utilization. In reference [5] the author presents work on review of different techniques of FM0, Manchester and Miller Encoding. These papers design the work strategy of complete circuits of Manchester, Miller, FM0, and FSM and also represent the study of compression to all the technique.

In [6] work proposed to encode the techniques of both the FMO and Manchester by the SOLS techniques. These techniques are used to eliminate the limitations of hardware by the utilization of two core technique which is (a) Compact of Area retiming (b) Sharing of Logic Operations. The numbers of transistor are used to reduce by using the compact of area retiming techniques up to 22 transistors. The logic sharing operations combine both the FMO and Manchester encoding. It used to operate at maximum frequency of both Manchester and FMO encodings at 2 GHz, 900MHz with the consumptions of power 1.58mW, 1.14mW respectively. In [7] this paper presents the review on academic background of both FM0 and Manchester and explains the usefulness of both the FM0 and Manchester encoding. This will also give the details for using DSRC. In DSRC signals consistency and DC-Stability are the requirements of the designing which help to fulfil the demands of both the FM0 and Manchester encoding technique.

In [8, 15, 22] author presents the work on design of architecture of a fully reused VLSI using the SOLS for both the technique of FM0 and Manchester encodings. The variety of coding techniques between FM0, Manchester and Miller encoding causes the restriction of the hardware utilization in VLSI architecture design. The limitation of hardware utilization eliminates by the SOLS techniques which have two core techniques such as area compact retiming and balance logic-operation sharing techniques. The techniques of Area-compact retiming are used to decrease the hardware problem like numbers of transistor and by the other techniques of balance logic operations sharing the helps for recognizing the logic components which may efficiently combines with the FM0 and Manchester encoding techniques. Each section activates the FM0 and Manchester encoding techniques. It will considerably recover the utilization of hardware at the rate of 100% and it also reduces the consumption of power. Both the FM0 and Manchester encoding techniques0 design to attain the high speed and fully reconfigured VLSI design architecture for the system application. The future scope of designing is used to implement by using the high performance of the FPGA devices.

In [10, 19] work proposed to overcome the techniques for utilization of hardware by using the SOLS technique of VLSI. It will used to design the DSRC (dedicated short-range communication). The DSRC standards are typically adopting for both FM0 and Manchester code encoding techniques to succeeding the dc-balance and enhancing the signal irresponsibleness. All the diversity coding between both the FM0 and Manchester codes limit the ways of potential to style the completely reused VLSI design. The utilization of hardware by SOLS techniques to recover the rate of utilization from 14% to 100% for each both FM0 and Manchester encoding.

In [11-12, 16, 24] the paper presents the work on review of DSCR system for the estimation of different form. Now a day the DSRC is the short-range wireless option which provides the low latency, Network achievement, when required. It presents the High dependability; provide the precedence for Safety Application, Interoperability, safety and Privacy. These are the challenging tasks which are faced by all. The article of Dedicated Short Range Communications (DSRC) deals with the applications for ITS. The wireless organizations are focused on economic assessment like vehicles communication; mobile Communications etc.

In [13] author proposed overcome technique of utilization of hardware by using the SOLS technique of the VLSI which is used to design the DSRC (dedicated short-range communication). The DSRC standards typically adopt both FM0 and Manchester codes encoding technique used for succeeding the dc-balance and enhancing the signal irresponsibleness. Rest all the diversity coding between both the FM0 and Manchester codes limits the way of potential to style the completely reused VLSI design for each. This paper is not only developed for the fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing work. [14] Proposed design is implemented to overcome the limitation of the existing design. The performance of design is implemented in Microwind and DSCH. To give an objective evaluation, the proposed VLSI architecture is implemented in full-custom design flows and FPGA design flow.

In [17] author proposed a system to minimize the problems of coding-diversity between both FM0 and Manchester that causes the restriction of hardware utilization of VLSI architecture design. In this paper, the fully reused VLSI architectures by using the SOLS technique for both FM0 and Manchester encodings are proposed. Area compact retiming and balance logic operation sharing are the two core techniques that are used to eliminate the limitation on hardware utilization by reducing the number of transistors and by combining the resources of both the FM0 and Manchester encoding. This paper is realized in180nm technology with outstanding device efficiency. The power Consumption is 29392.843nW for both the Manchester encoding and FM0 encoding.

In [20, 25] author proposed a system to minimizing the problem of coding-diversity between FM0 and Manchester encodings that causes the limitation on hardware utilization of VLSI architecture design. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. Area compact retiming and balance logic operation sharing are the two core techniques that are used to eliminate the limitation on hardware utilization by reducing the number of transistor and by combining the resources of FM0 and Manchester encodings. It will balance the logic operation for sharing which is efficiently combines with the FM0 and Manchester encodings with the identical logic components.

In [21] author proposed a method of utilization of VLSI architecture for reduction of power by using both the FM0 and Manchester encoding. By reducing the number of components to reduce the use of power and improves the performance of both the FM0 and Manchester encoding. The results are being observed by using the spice. For Manchester encoding the consumption of power is 0.72 mw. The consumptions of power are 0.14 mw for FM0 encoding. Both the FM0 and Manchester encoding techniques are widely used to contribute the short range communication. Reliability of signal is attaining by DSRC for adopting both the FM0 and Manchester encoding.

In [22] the performance of this paper is evaluated on Xilinx FPGA Spartan-3E kit. It interfaces with CMOS, TTL or N channel support circuitry. These encoding techniques generally works at transistor level hence the transmitted signal reach with dc-balance, enhance the signal reliability. In existing works the design has the limitation that it does not support fully reused VLSI architectures. To rectify these problems, the FM0 and Manchester encoders are designed with SOLS technique to achieve high speed and fully reused VLSI architectures for DSRC application systems. The performance of this paper is implemented on post layout simulation in 45nm CMOS technology. This model not only supports fully reused architecture but also provides high performance.

In [23] author the paper present the diversity coding techniques between the FM0 and Manchester encoding. It causes the limitation of the hardware utilization by using the VLSI architecture design. The encoding technique of both the FMO and Manchester fully reused by using the SOLS techniques are proposed. It eliminates the limitations of utilization of hardware. To reduce the transistor counts by using the ACR techniques to reposition the hardware resource. The BLOS combine the FM0 and Manchester encoding with the identical logic component. By the SOLS techniques the hardware's improve rate is of 57.14% to 100% for both the technique of FM0 and Manchester encoding. The hardware balanced architectures are used to understand by the different CMOS technologies. This paper are not only develops the fully reused VLSI architecture, but it also exhibit the well-organized performances which compared with the existing work.

In [26] author proposed SOLS technique to prevent the wide range of code diversity that limits the hardware utilization rate of such a reusable encoder. To implement the system which has its own advantages like smooth traffic control, vehicular safety etc for DSRC communication protocol is used in this system to encode the message and transmit it to other DSRC. The data is encoded by using FM0 and Manchester encoding that causes the problem and can be overcome by using SOLS technique. The SOLS encoder is used for the better advantages than use the normal reusable encoder in term of device utilization. Besides the logic delay and memory usage of the system also get reduced.

In [27] author shows to solve the problem by using the SOLS technique which introduced to solve the utilization of hardware problem caused at the time when both the FM0 and Manchester encoding is used to encode the message in DSRC. By the two parameters we are mainly used for the area compact retiming and balance logic-operation sharing. By using these parameter it will reduces the hardware setup problems by reducing transistor and it also combines the FM0 and Manchester encodings which is identical to the logic components respectively.

In [28] author proposed a system to minimize the problems of coding-diversity between both FM0 and Manchester that causes the restriction of hardware utilization of VLSI architecture design. In this paper, the fully reused VLSI architectures by using the SOLS technique for both FM0 and Manchester encodings are proposed. Area compact retiming and balance logic operation sharing are the two core techniques that are used to eliminate the limitation on

hardware utilization by reducing the number of transistors and by combining the resources of both the FM0 and Manchester encoding. This paper is realized in180nm technology with outstanding device efficiency. The power Consumption is 29392.843nW for both the Manchester encoding and FM0 encoding.

3. CONCLUSION:

The design strategies of number of scholars exploit the present work and it presents a brief of it. Using similarities in the FM0 encoding and Manchester encoding techniques, hardware architecture is to be developed. Manchester and FM0 coding are very popular codes, as these codes are level insensitive, self-clocking and they provide signal absence detection and having the encoding clock rate embedded within the transmitted data. FM0 and Manchester encoding architectures combined together to form efficient compact architecture through SOLS. This review paper presents the common work which explains the entire circuits of FM0 encoder, Miller, Manchester and a FSM (finite state machine) for all three encoders which are designed by using VHDL (Verilog Hardware Description Languages). The concept of encoding will be used techniques in various applications as future work.

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