An E- Type Asymmetric Multilevel Inverter With Reduced Number of Switches.

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Abstract: This paper presents a new E-Type module for asymmetrical multilevel inverters with reduced components. Each module produces 13 levels with four unequal DC sources and 10 switches. The design of the proposed module makes some preferable features with a better quality than similar modules such as the low number of semiconductors switches and DC sources and low switching frequency. Also, this module is able to create a negative level without any additional circuit such as an H-bridge which causes reduction of voltage stress on switches. Cascade connection of the proposed structure leads to a modular topology with more levels and higher voltages. MATLAB simulations are presented to validate the proposed module good performance.

Key Words: Asymmetric, components, Matlab, E-Type, multilevel inverter, Power Converter.

1. INTRODUCTION:

Multilevel inverters (MLIs) have been in the focus for decades because of interesting features such as high quality output voltage, operation in high voltage/power, low stress on switches, etc.

Multilevel converters are different arrangements of semiconductor switches with DC links to create n-level output waveform. Multilevel converters have a wide range of applications which has rapidly developed the area of power electronics with good potential for further technology [1]. They can be used in photovoltaic systems, wind farms, and HVDC systems. They are divided into three main categories [2]: Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascade H-Bridge (CHB). In 1981, NPC was introduced as the first multilevel converter which can be used in medium voltage applications. Early 1990s, FC was presented and in 1996, CHB was reintroduced. Design of multilevel inverters depends on the number of voltage levels, number of semiconductors, output quality, number of DC supplies and DC link capacitors, THD amplitude, maximum voltage level, creating positive and negative level, modularity, switch stress and total standing voltage (TSV).

Researchers presented different types of modular multilevel inverters. As shown in Fig.1.a, each level is created by two switches and one source in [3]. These levels are connected in series together to achieve positive voltage levels and an auxiliary H-bridge circuit is used to create alternative voltage. Note that, H-bridge switches tolerate more voltages than other switches. As shown in Fig.1.b, the stress of H-bridge switches are divided between each submodule [4]. Two capacitors are added for each DC source to reach more voltage levels with the penalty of using more components. Researchers tried to reach more levels with lower components. Asymmetric multilevel inverters which have unequal DC links become interesting in order to increase the quality of output waveform by minimizing the number of components. Modules are designed based on optimal using of DC links by reduced switches.

One of the important factors of MLI design for high voltage applications is high voltage stress on the switches of the output H-bridge. Therefore, a redesign is vital to reduce the stress of the switches by dividing H-bridge voltage into all sub-modules in order to have a uniform stress on all switches which in turn leads to the increasing number of semiconductors and total standing voltage (TSV) of the module. This paper aims to achieve maximum capacity from DC link by a suitable arrangement of switches which improves economic implementation cost, switching frequency, TSV, number of levels, and THD. It presents a new asymmetric multilevel module based on cascade category which does not need any additional circuit to create negative voltage levels. Also, it makes 13 levels by reduced switches. The proposed system illustrates multilevel inverters including module description, switching patterns, cascade connection and comparison table with similar modules. Selective harmonic elimination (SHE) is also introduced for for eliminating harmonics.

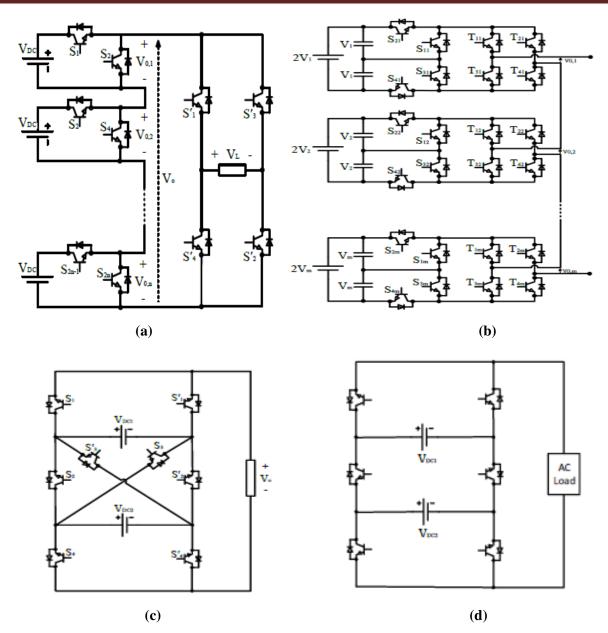


Fig.1 Some Modular multilevel inverter topologies

2. LITERATURE REVIEW:

A comparative study between the proposed topology and other famous ones is carried out regarding the number of semiconductors, DC links, capability to generate negative voltage level and the number of switches. Among these topologies are: NPC, FC, CHB. According to Table I, the number of semiconductors (switches and diodes), number of DC links are reduced down to 5(NL-1)/6 and (NL-1)/3 respectively which are lower than other topologies. Note that this topology can generate a negative voltage level which does not need any additional circuit. This ability along with lower components and stress on the devices confirms that the proposed inverter can perform well in comparison with other existing ones.

TABLE I
Comparison Of Some Modular Multilevel Inverter Topology

	NPC	FC	СНВ	PROPOSED (E -Type)
No. of switches	2(N _L -1)	$2(N_L-1)$	$2(N_L-1)$	5(N _L -1)/6
No. of Diodes	N _L +1	$2(N_L-1)$	$2(N_L-1)$	5(N _L -1)/6
No. of DC links	$(N_L-1)/2$	(N_L-1)	$(N_L-1)/2$	$(N_L-1)/3$
Negative level	With at least two	With at least two	With H bridge	Inherent
	arms	arms		

3. METHODOLOGY:

A general schematic diagram of a typical asymmetrical multilevel inverter with two DC links for description of multilevel operation is shown in Fig 2. Unequal DC links can be arranged with different connections (through switching components) in order to achieve high number of voltage levels.

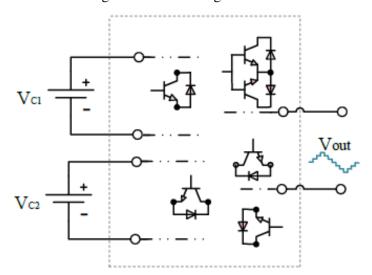
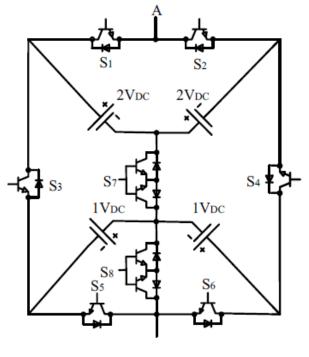


Fig.2 The general structure of asymmetric multilevel inverters

For example, assuming VC1=VDC and VC2=2VDC voltage levels of $\pm VDC$ $\pm 2VDC$ and $\pm 3VDC$ can be achieved by choosing suitable paths from switches and DC links depends on the module topology. Using this idea for multilevel inverters, a different ratio of DC link voltages may be utilized to generate a different number of output voltage levels. An elimination in harmonic content peak with a same switching frequency and the same structure is approximately expected by increasing the number of output voltage levels in the asymmetrical inverter.

Module Configuration:

This proposed system introduces a new topology of asymmetric multilevel modular with a new component arrangement including 10 switches, 10 diodes and 4 unequal DC sources (two 2VDC, two 1VDC) named as Envelope type (E-Type). This arrangement synthesizes voltage sources produces 13 levels (6 positive level, 6 negative level and zero level) without any additional circuit. The main concept of this circuit is to create different paths from different sides of a DC source to be connected to other sources. Fig.4 shows the configuration of E-Type asymmetrical module in where DC sources are located in the middle of the circuit and are connected together to form different voltage levels via surrounding switch (S1-S6). A bidirectional switch (S7) is required to avoid short circuit of DC sources on left or right sides of the module. Another bidirectional switch (S8) is also needed to achieve voltage levels of ± 5 . Different switching conditions of this structure are shown in Fig.3 and Table I.



(a) Circuit topology

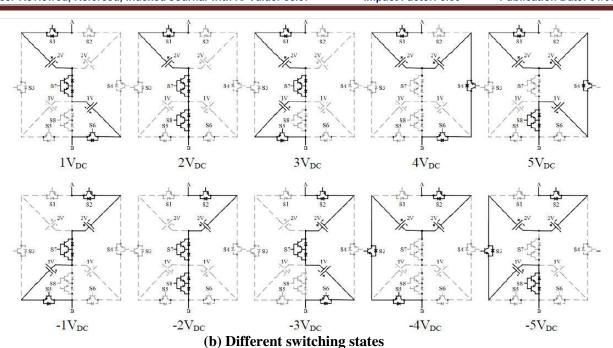


Fig. 3 Proposed E-Type module of multilevel inverter

TABLE II SWITCHING TABLE

		S1	S2	S3	S4	S5	S6	S7	S8
level	$1V_{DC}$	1	0	0	0	0	1	1	0
	2V _{DC}	1	0	0	0	0	0	1	1
e le	3V _{DC}	1	0	0	0	1	0	1	0
positive	4V _{DC}	1	0	0	1	0	1	0	0
iso	5V _{DC}	1	0	0	1	0	0	0	1
<u>d</u>	6V _{DC}	1	0	0	1	1	0	0	0
75	-1V _{DC}	0	1	0	0	1	0	1	0
level	-2V _{DC}	0	1	0	0	0	0	1	1
	-3V _{DC}	0	1	0	0	0	1	1	0
ativ	-4V _{DC}	0	1	1	0	1	0	0	0
Negative	-5V _{DC}	0	1	1	0	0	0	0	1
Z	-6V _{DC}	0	1	1	0	0	1	0	0

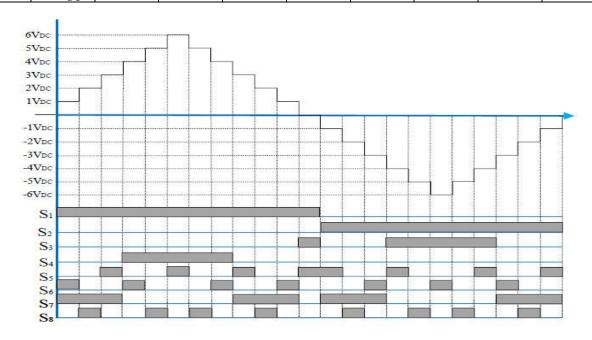


Fig.4 Switching Pattern Of Proposed Converter In One Cycle

As shown in Table II, switch pairs (S1, S4) and (S2, S3) belong to positive and negative levels, respectively. In addition, (S1, S2) and (S3, S4) cannot be on at the same time. Fig.4 shows output voltage of the proposed inverter with the associated pulse pattern in one cycle of fundamental voltage. As shown in Fig.4, switches S1, S2, S3, S4 and S7 are turned on and off in low frequency which reduces switching losses to a great extent. Other switches also operate in a reasonable switching frequency. Table II shows number of voltage levels, semiconductor components, DC sources and drivers based on number of module units (n) and number of desired levels (NL).

TABLE III EQUATIONS OF E-TYPE MODULE

	Based on number of module units	Based on number of desired levels
Levels	12n+1	$N_{\rm L}$
Number of switches	10n	5(N _L -1)/6
Number of Diodes	10n	5(N _L -1)/6
Number of DC Links	4n	$(N_L-1)/3$
TSV	20n	10(N _L -1)/6

Number of levels are in the form of 12n+1 (n=1, 2, 3, ...)

Fig.3(b) shows all switching states of E-type module. The designing of the proposed module and their switching paths are smartly selected in such a way that there are no positive pole of DC links on the anode side of diode to conduct. Thus, diodes prevent short circuiting of the switches. Also Fig.3(b) illustrates the switching paths does not form any close loop for DC links. It guarantees that short circuiting will be not occurred in E-type module.

For proposed topology, as shown in Fig.5, there are 6 voltage levels in a quarter-wave symmetry and therefore 6 switching angles (α i) have to be calculated. Third harmonic multiples are eliminated in three phase systems.

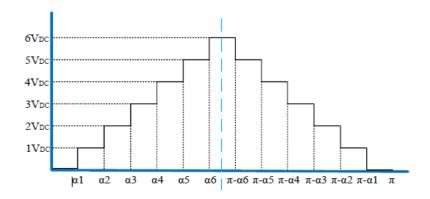
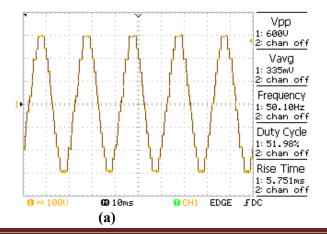
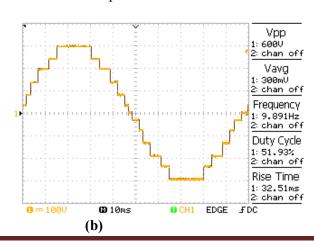


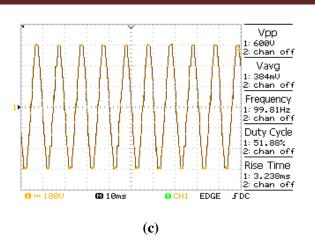
Fig.5 Shows the waveform of Selective harmonic elimination modulation to find αi (Quarter wave symmetry)

4. SIMULATIONS RESULTS:

Experimental results are carried out to verify the results of simulation and analysis in order to achieve a 13-level sinusoidal waveform. Each level is considered 50 volts, and thus there are two 50 volts and two 100 volts DC sources. Fig.6 depicts voltage waveform of the proposed E-Type module for 10 Hz (Fig.6.a), 50 Hz (Fig.6.b) and 100 Hz (Fig.6.c). FFT analysis for one cycle is illustrated in Fig.6.d where THD of experimental waveform is 4.54%.







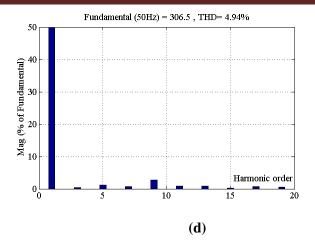


Fig.6 Output voltage and FFT analysis of proposed multilevel

5. CONCLUSION:

This paper presented a new multilevel inverter topology named as Envelope Type (E-Type) module which can generate 13 levels with reduced components. As E-Type module can be easily modularized, it can be used in cascade arrangements to form high voltage outputs with low stress on semiconductors and lowering the number of devices. Modular connection of these modules leads to achieve more voltage levels with different possible paths. It causes an improvement in the reliability of the modular inverter which enables it to use different paths in case of malfunction for a switch. The main advantage of proposed module is its ability to generate both positive and negative output voltage without any H-bridge circuit at the output of the inverter. Also module is tested in three frequencies and under different loads which results shows good performance.

REFERENCES:

- 1. R. Feldman, M. Tomasini, E. Amankwah, J.C. Clare, P.W. Wheeler, D.R. Trainer, R.S. Whitehouse, "A Hybrid Modular Multilevel Voltage Source Converter for HVDC Power Transmission,", IEEE Trans. Ind. Appl., vol.49, no.4, pp.1577–1588, July-Aug. 2013..
- 2. J. Rodriguez, J.S. Lai and F.Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. on Power Electron., vol. 49, no. 4. pp. 724–738, Aug. 2002.
- 3. E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," Elsevier J. Energy Convers.Manage, vol. 50, no. 11, pp. 2761–2767, Nov. 2009.
- 4. Emad Samadaei, S.A. Gholamian, Sheilhoeslami, J. Adabi "An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverter With Reduced Components", IEEE transaction on industrial electronics. 2015
- 5. E. Babaei, M.F. Kangarlu, M. Sabahi, "Extended multilevel converters: an attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters" IET Power Electron., Volume 7, Issue 1, p. 157–166, Jan. 2014.
- 6. M. FarhadiKangarlu, E. Babaei, "Cross-switched multilevel inverter: an innovative topology," IET Power Electronics, vol.6, no.4, pp.642–651, Apr. 2013
- 7. Y. Ounejjar, K. Al-Haddad, L.-A.Grégoire, "Packed U Cells Multilevel Converter Topology: Theoretical Study and Experimental Validation" IEEE Trans. Ind. Electron., Vol. 58, no.4, P.1294–1306, Apr. 2011.
- 8. A. Mokhberdoran, A. Ajami, "Symmetric and Asymmetric Design and Implementation of New Cascaded Multilevel Inverter Topology," IEEE Trans. on Power Electron., vol.29, no.12, P.6712–6724, Dec. 2014.
- 9. Ralph Feldman, Matteo Tomasini, Emmanuel Amankwah, Jon C. Clare. "A Hybrid Modular Multilevel Voltage Source Converter for HVDC Power Transmission" IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, VOL. 49, NO. 4, P.1577-1588, JULY/AUGUST 2013.