

Simulation and Analysis of Three-Phase Five-Level Grid Connected Diode-Clamped Multilevel Inverter

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Abstract: Multilevel inverter has become attractive in the power industries and it can be applied in many applications especially in renewable energy systems and improvement of the power quality. In this article, 10 MW three-phase five-level diode clamped grid connected multilevel inverter was constructed by simulation. The proposed multilevel inverter used a carrier based sinusoidal pulse width modulation (SPWM) scheme in order to produce the desired output voltage. The scheme is the modulation of three identical reference signals which is 120° phase shifted to each other comparing to a 5 kHz carrier signal. These reference signals comprise of some harmonics in order to generate a SPWM signal for switches in the inverter. A phase lock loop (PLL) was utilized together with the controller in order to phase and frequency locking between the voltage at the point of common connection (PCC) and voltage at the grid system. After the proposed inverter connected to the grid system, it can be injected the inverter current into grid system by using the appropriated PI (proportional-integrator) controller within the control scheme. However, LCL filter was also utilized at the inverter output for reducing harmonics contents. It results to reduce the output harmonic contents. In which, the value of total harmonic distortion (THD) at PCC is less than 5%. Some advantages that multilevel inverters are minimum harmonic distortion, reduced EMI generation and operation on several voltage levels. In this paper, grid-connected three-phase five-level diode clamped multilevel inverters (DCMLI) was analysed and simulated.

Key Words: Diode Clamped Multilevel Inverter, Total Harmonic Distortion, SPWM, phase lock loop.

1. INTRODUCTION:

Nowadays, the power obtained from solar and wind energy are connected to the grid for better utilization of renewable energy sources. Electrical energy that flows from the renewable energy source into the grid system depends on the limitation of the storage systems and efficiency of the inverter. The power extraction from renewable energy sources cannot be directly utilized by the load or the grid. The power electric interface such as DC-DC converters and DC-AC inverters especially MLIs are used as an interface between them. The utilization of the topologies of the grid inverter depends on the type of such renewable energy source. However, the applications of sources in grid system such as solar, fuel cell or wind turbines are affected in design and operation of that grid network. Multilevel inverters are suitable for high voltage and high power application because of less harmonic spectrum output voltage that results into a better synchronization [1].

The three-phase grid connected multilevel inverter is compared with the three-phase conventional inverter and the observed THD of the conventional inverter is 31% and THD of MLI output voltage is analysed which is 0.13% that found to be very less compared to six pulses conventional inverter topologies [2]. Grid connected inverters are more complicated and use switching devices (IGBT and MOSFET) that can control the switch-on and switch-off time and adjust the output signal to that of the grid [3]. Using multilevel inverters in such grid connected PV system considerably reduces the THD level of the current injected into the grid [4]. Novel multilevel inverter topology generates a high-quality output voltage waveform with lower order THD of output voltage and current and hence which is suitable for renewable energy sources interfacing to AC grid [5]. An 11 kV series connected H-Bridge MLI is proposed to achieve a compact and light direct grid connection of renewable energy system [6]. The THD content in the grid or infinite bus current in three-level inverter based system is 5.93% while in two-level inverter system is 197.67% so a large difference in the level of distortion at the same input provided to the system [7]. The multilevel line commutated inverter topology has been proposed and analysed which improves the wave shape and hence reduces the THD of the line current in a grid tie line commutated inverter [8]. If the DCMLI runs under PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high voltage high power applications [9]. With a capacitance connected in parallel with the renewable energy source, the MLI can provide static var compensation even when there is no output power from the photovoltaic or fuel cell energy source [10].

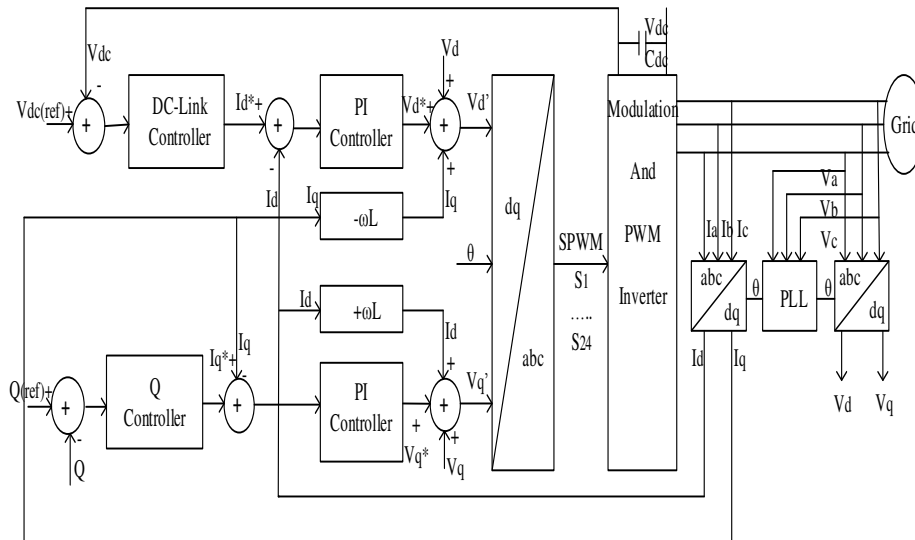


Fig.1 Block Diagram for Synchronous Rotating Reference Frame Control Structure of grid connected inverter

In this article, the diode clamped topology was used in three-phase five-level grid connected inverter. However, various strategies of modulation techniques and control schemes were implemented in multilevel diode clamped grid connected inverter system. The sinusoidal pulse width modulation is the useful technique for providing an appropriate output voltage waveform of such multilevel inverters. In order to synchronize the inverter's output to the grid system at PCC, the frequency and phase of PCC voltage were detected by phase lock loop (PLL). The control scheme of the grid connected inverter is shown in Fig. (1).

2. COMPONENTS OF GRID CONNECTED MULTILEVEL INVERTER:

2.1 Three-Phase Five-Level Diode Clamped Multilevel Inverter

The Multilevel Inverter with a large number of steps can generate high quality waveforms. This inverter generates near sinusoidal output voltage and as a result has very low harmonic contents. The three phase diode clamped multilevel inverter is the common multilevel inverter used for various application. So, the three phase diode clamped multilevel inverter is adopted in this paper. Each phase leg of the five-level inverter has four pairs of switching devices in series. The centre of each device pair is clamped to the neutral through clamping diodes. The output obtained from five-level inverter is a quasi-square wave output if fundamental frequency switching is used. For three-phase five-level DCMLI case, a total of 24 switches and 18 diodes of equal voltage rating are used. A M-level inverter requires (M-1) storage capacitors, 6x(M-1) switches and 6x(M-2) clamping diodes where M is the total number of positive, negative and zero levels in the output voltage.

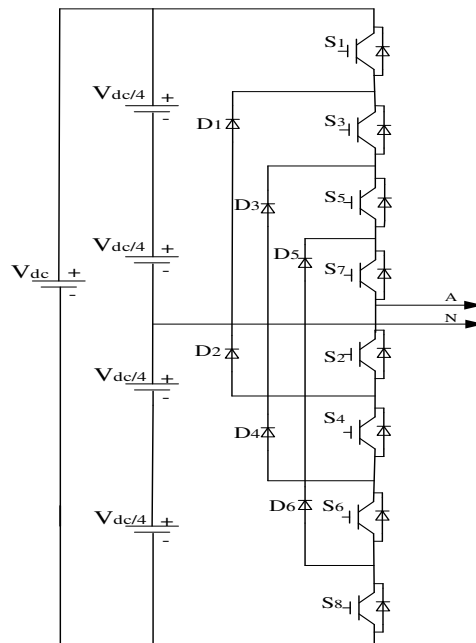


Fig.2(a) Block Diagram for One Leg of Three-Phase Five-Level DCMLI

Fig.2(a) shows one leg of three-phase half-bridge five-level diode clamped inverter. For five-level inverter, the order of numbering of the switches for phase A is $S_1, S_2, S_3, S_4, S_5, S_6, S_7$ and S_8 . The DC bus consists of four capacitors acting as voltage divider. For a DC bus voltage V_{dc} , the voltage across each capacitor is $V_{dc}/4$ and voltage stress on each device is limited to $V_{dc}/4$ through clamping diode. Table.1 shows the output voltage levels and the corresponding switching states for one phase of five-level DCMLI. The switches are arranged into 4 pairs (S_1, S_2), (S_3, S_4), (S_5, S_6) and (S_7, S_8). If one switch of the pair is turned on, the complementary switch of the same pair must be off. Four switches are triggered at any point of time to select the desired level in the DCMLI. Fig.2(b) represents the PWM generation technique for five-level DCMLI.

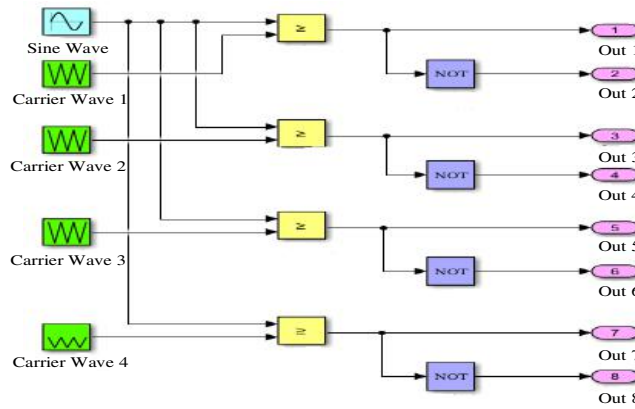


Fig.2(b) PWM Generation Using PD-PWM Technique for Five-Level Inverter

TABLE I
 Switching States for One Leg of Three-Phase Five-Level DCMLI

S_1	S_3	S_5	S_7	S_2	S_4	S_6	S_8	V_{an}
1	1	1	1	0	0	0	0	$V_{dc}/2$
0	1	1	1	1	0	0	0	$V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

The steps to synthesis the five-level phase A output voltage in TABLE I are as follows:

- 1) For an output voltage of $V_{an} = V_{dc}/2$, all upper switches S_1, S_3, S_5 and S_7 are turned on.
- 2) For an output voltage of $V_{an} = V_{dc}/4$, three upper switches S_3, S_5, S_7 and one lower switch S_2 are turned on.
- 3) For phase A output voltage of $V_{an}=0$, two upper switches S_5, S_7 and two lower switches S_2, S_4 are turned on.
- 4) For an output voltage of $V_{an} = -V_{dc}/4$, one upper switch S_7 and three lower switches S_2, S_4, S_6 are turned on.
- 5) For an output voltage of $V_{an} = -V_{dc}/2$, all lower switches S_2, S_4, S_6 and S_8 are turned on.

The phase A output voltage V_{an} has five states; $V_{dc}/2, V_{dc}/4, 0, -V_{dc}/4$, and $-V_{dc}/2$.

2.2. Modulation Techniques

Several modulation techniques are developed for multilevel inverters. The commonly used modulation techniques are sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM) and selective harmonic elimination pulse width modulation (SHEPWM). Among them, SPWM is very simple control method and less switching losses for multilevel inverter. In SPWM, a sinusoidal waveform is related to a carrier waveform to get gate pulses of the switches to an inverter. M-level output desires (M-1) carrier per the common multilevel inverter.

2.3. Harmonic Filter

The harmonic filters are used for improving the sinusoidal waveform of the output voltage of AC test systems. Both switching frequency effects and grid voltage distortion can lead to poor power quality. Switching noise and high frequency harmonics are usually attenuated by inductors and capacitors. Filters are main part of a grid connected

renewable energy system. A well designed filter can attenuate switching frequency components but impacts on control bandwidth and the impedance presented to grid distortion. LCL-Filter has the best design to filter the harmonics for grid connected renewable energy systems. Fig.3 shows these LCL filter configuration circuit.

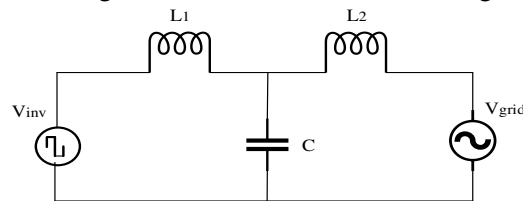


Fig.3 LCL Filter Configuration Circuit

The LCL-Filter represents a suitable compromise for the system intended for use in the research. The LCL-Filter can give sufficient output performance with a 5 kHz carrier frequency. The calculation of the LCL-Filter is given in the following equations. The ripple current can be chosen as 0.15 to 0.25 of rated current.

$$\Delta I_{1\max} = \frac{V_{dc}}{8L_2f_{sw}} \leq 0.2I_{rated} \quad (1)$$

$$L_1 = (4\sim 6) \times L_2 \quad (2)$$

$$Q_c = 3 \times (2\pi f_1) \times C V_{rated}^2 \leq 5\% P_{rated} \quad (3)$$

In these equations $\Delta I_{1\max}$ is the ripple current, V_{dc} is DC input voltage, L_1 and L_2 are filter inductances, C is filter capacitance, f_{sw} is switching frequency, f_1 is fundamental frequency, I_{rated} is rated current of grid, V_{rated} is rated voltage of grid, P_{rated} is rated power of grid and Q_c is absorbed reactive power by capacitor.

Cut-off frequency, sometimes also known as break frequency or corner frequency is a boundary in the system frequency response at which energy flowing through the system begins to be reduced rather than passing through. The attenuation characteristics at the cut off frequency (f_c) is one of the critical factors involved in designing a third order filter. The switching frequency in high power applications is chosen with regard to inverter efficiency, since switching losses are significant portion of the overall losses. These frequencies can be calculated by using the equations (4), (5) and (6).

$$f_c = f_{sw}/10 \quad (4)$$

The resonant frequency should be;

$$10f_1 < f_0 < 0.5f_{sw} \quad (5)$$

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \quad (6)$$

Where, f_c is cut off frequency, f_{sw} is the switching frequency and f_0 is the resonant frequency. The current and voltage harmonic levels are the main requirements of output filter design.

3. CONTROL STRATEGIES OF GRID SYNCHRONIZATION:

There are several different forms of control strategies of grid connected multilevel inverter depending on the reference frame chosen, such as stationary reference frame (SRF), synchronous rotating reference frame (SRRF), rotor reference frame (RRF) and arbitrary reference frame (ARF). The SRRF method also called dq control is widely used in three-phase system. The major different between the SRF and SRRF is that most SRF suffers from an arbitrary to eliminate steady-state error. However, the SRRF method solves this problem, these frame is more complex and requires pathways for each of orthogonal components in order to apply Park Transformation. The SRRF regulator has many advantages for the three-phase grid-tied inverter.

- Time invariant control variables and fast response in case of load change.
- Controller design is similar to that used with a conventional DC to DC converter, zero state error at steady-state and easy filtering.
- Decoupling of the control of active and reactive power. This leads to the ability to control amplitude and phase separately.
- Potentially a high controller gain at the fundamental frequency.
- The voltage feed-forward terms allow a wider PI controller gain choice and wider number range for the integrators.
- Improvements to the dynamic response.
- Improvements to the anti-islanding detection zone.

Synchronization is one of the most important issues in the control of power electronics equipment connected to the grid. The synchronization between inverter and grid means that both will have the same phase angle, frequency and voltage magnitude. Grid synchronization methods are used so far such as: zero-crossing method, filtering of grid voltages, phase lock loop, etc. A conventional method of grid synchronization for grid connected DC/AC inverter is to duplicate the grid voltage so that output current reference has the same phase as the grid voltage. This method of grid synchronization cannot provide inverters the ability of controlling reactive power flow.

3.1. Phase Lock Loop (PLL)

PLL is the most modern and most common method for determination of phase angle and frequency of the grid voltage. Synchronization of inverter with the grid line is done by PLL. As started earlier, the PLL computes the rotation frequency of the grid voltage by first transforming it to the dq frame and then force the quadrature component of the voltage to zero to eliminate cross coupling in the active and reactive power terms. A proportional (k_p) and integral (k_i) gains of the controller were set through an iterative process to achieve a fast settling time. In three-phase systems, the PLL usually employs a Synchronous Rotating Reference Frame (SRRF-PLL). In spite of its good factors under ideal voltage conditions, the response of the SRRF-PLL can become unacceptably when the utility voltage is unbalanced. Fig.4 shows the schematic diagram of the PLL.

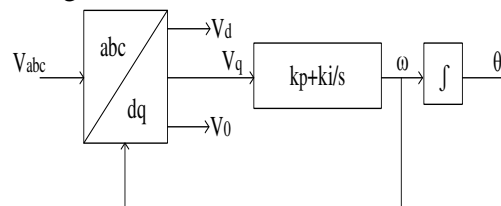


Fig.4 Schematic Diagram of Phase Lock Loop (PLL)

$$\omega = k_p v_q + k_i \int v_q dt \tag{7}$$

$$\theta = \int \omega dt \tag{8}$$

Where, k_p is the proportional gain of controller, k_i is the integral gain of controller, ω is the angular rotation frequency and θ is the rotation angle .

The dq transformation is used to transform three-phase system quantities like voltages and currents from the synchronous reference frame (abc) to a synchronous rotating reference frame (dq) with three constants components when the system is balanced.

$$\begin{bmatrix} X_d \\ X_q \\ X_0 \end{bmatrix} = \mathbf{T} \times \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{9}$$

$$\mathbf{T} = \frac{\sqrt{2}}{\sqrt{3}} \times \begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{10}$$

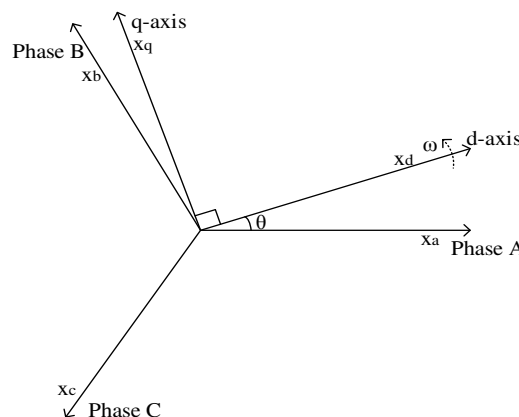


Fig.5 Phasor Diagram of abc and dq Reference Frame

X can be either a set of three-phase voltages or currents to be transformed, T is transformation matrix and ω is the angular rotation frequency of the frame. The angle between the direct axis (d-axis) and phase (a-axis) is defined as θ . An overview of the dq transformation and sinusoidal PWM technique are presented for their importance in building the inverter control system.

3.2. DC-Link Controller

The grid side converter control system is developed to regulate the grid voltage by regulating the DC-link voltage V_{dc} . The control system is assessed based on the quality of the injected AC current into the grid so as determined by the THD limits specified by the IEEE Std. (929-2000). A DC-link capacitor is used after the DC converter and acts as a temporary power storage device to provide the voltage source inverter with a steady flow of power. The capacitor's voltage is regulated using a DC-link controller that balances input and output powers of the capacitor. The voltage source inverter is controlled in the rotating dq frame to inject a controllable three-phase AC current into the grid. To achieve unity power factor operation, current is injected in phase with the grid voltage. The control option for grid interface is aimed to adjust the active power and reactive power delivered to the grid. The control system uses two control loops, these are an external control loop which regulates DC-link voltage and an internal control loop which regulates I_d and I_q grid currents. So, the DC-link controller is the external control loop. I_d current reference is the output of the DC voltage external controller and I_q current reference is set to zero in order to maintain unity power factor. Fig. 6 shows the DC-link controller.

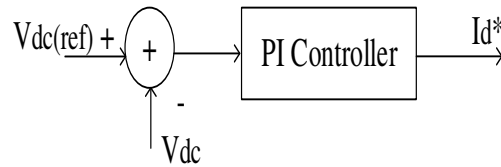


Fig.6 Schematic Diagram of DC-Link Controller

$$V_{dc - error} = V_{dc - ref} - V_{dc} \tag{11}$$

$$I_d^* = k_p - v_{dc}(V_{dc - error}) + k_i - v_{dc} \int (V_{dc - error})dt \tag{12}$$

$$I_q^* = 0 \tag{13}$$

Where, V_{dc} is the DC-link voltage, V_{dc-ref} is the reference DC-link voltage, $V_{dc-error}$ is the DC-link voltage error, I_d^* is the d-component of grid current, I_q^* is the q-component of grid current, $k_p - v_{dc}$ is the proportional gain of PI controller and $k_i - v_{dc}$ is the integral gain of PI controller.

3.3. dq Current Controller

The dq current controller is the internal control loop. I_d^* is drawn from DC-Link controller and compared with the d-axis component of grid current. The compared signal is processed through the PI controller for minimizing the error. Similar process is adopted for the q-axis component and then I_q^* is considered as zero. The outputs of the PI controllers are processed through the saturation block, so that the errors cannot exceed the upper or lower limits. V_d^* is drawn from PI controller and compared with d-axis component of grid voltage. V_q^* is also drawn PI controller and compared with q-axis component of grid voltage. V'_{dq} generated by the voltage regulator is converted into the three-phase by the transformation reference frame and then the reference voltage acts as a control signal for the PWM generator. The generated switching pulses are able to control the inverter output voltage according to the grid voltage.

$$V_d^* = k_p - gc - CR(I_d^* - I_d) + k_i - gc - CR \int (I_d^* - I_d)dt \tag{14}$$

$$V_d' = V_d^* - (L_{grid}\omega I_q) + V_d \tag{15}$$

$$V_q^* = k_p - gc - CR(I_q^* - I_q) + k_i - gc - CR \int (I_q^* - I_q)dt \tag{16}$$

$$V_q' = V_q^* + (L_{grid}\omega I_d) + V_q \tag{17}$$

Where in these equations, $K_{p-gc-CR}$ is the proportional gain of PI controller, $K_{i-gc-CR}$ is the integral gain of PI controller, V_d^*, V_q^* are the reference dq components of the grid voltage, I_d, I_q are the dq axis components of grid current by using park transformation (abc to dq), V_d, V_q are the dq-axis components of grid voltage, V_d', V_q' are the dq components voltage sensed to the inverter, L_{grid} is the grid side coupling inductance and ω is the rotation frequency. By applying modulation index and phase conversion to V_d' and V_q' , the values of V_d and V_q are obtained. Then by using park transformation, the control voltage $V_{grid-control}$ is calculated and used for generating PWM signals for grid side inverter.

4. SIMULATION STUDY OF GRID CONNECTED THREE-PHASE FIVE-LEVEL DCMLI:

The role of three-phase five-level grid connected MLI is to improve power quality of grid tied renewable energy system by reducing THD and increasing the voltage level. The inverter handles output current regulation and DC bus voltage regulation. For this the DC link voltage must be kept greater than the peak value of the grid voltage. The DC-link voltage V_{dc} was controlled in the inverter by using PI controller. The DC-link voltage is compared with the reference value and the error is fed into the PI controller, which subsequently tries to reduce the error. In this way V_{dc} can be maintained at a value greater than the peak value of the grid voltage. The minimum DC-link voltage $V_{dc(min)}$ for multilevel inverter necessary to achieve an output line to line voltage $V_{ll(rms)}$ of 11 kV can be calculated from equation (18).

$$V_{dc(min)} = \frac{\sqrt{2} \times V_{ll(rms)}}{(M - 1)} \tag{18}$$

To determine the nominal DC-link voltage of the inverter, a voltage reserve of 20% is assumed. So, the nominal DC-link voltage becomes;

$$V_{dc(nom)} = 1.2 \times V_{dc(min)} \tag{19}$$

In these equations, $V_{dc(min)}$ is the minimum DC-link voltage, $V_{ll(rms)}$ is the RMS value of line to line grid voltage, $V_{dc(nom)}$ is the nominal value of DC-link voltage and M is the number of inverter level.

For delivering energy properly to the grid, the frequency and phase of the inverter should be same as that of the grid voltage. Therefore, a proper grid synchronization method is necessary. For this a PLL is used in the control system so as to generate a reference current which is in phase with the grid voltage. The current injected into the grid ie, the grid current is compared with the reference grid current and the error is fed into the PI current controller. The output of the PI controller is compared with a triangular signal so as to obtain switching pulses to the inverter. Simulation model of of grid connected three-phase five-level DCMLI is shown in Fig.7 and control system of these model is shown in Fig.8. Moreover, the simulation parameters of the proposed system are given in Table. 2.

TABLE I
 Design Parameters of Grid Connected Five-Level DCMLI for Simulation

Parameters	Specification
DC-Link Voltage (V_{dc})	18.66762 kV
Switching Frequency (f_{sw})	5 kHz
Cut Off Frequency (f_c)	200 Hz
Fundamental Frequency (f_m)	50 Hz
Line to Line Grid Voltage (V_{ll})	11 kV(AC)
Rated Power (P)	10 MW
Filter Inductance (L_1)	22.2295 mH
Filter Inductance (L_2)	4.446 mH
Filter Capacitance (C)	7.892 μ F

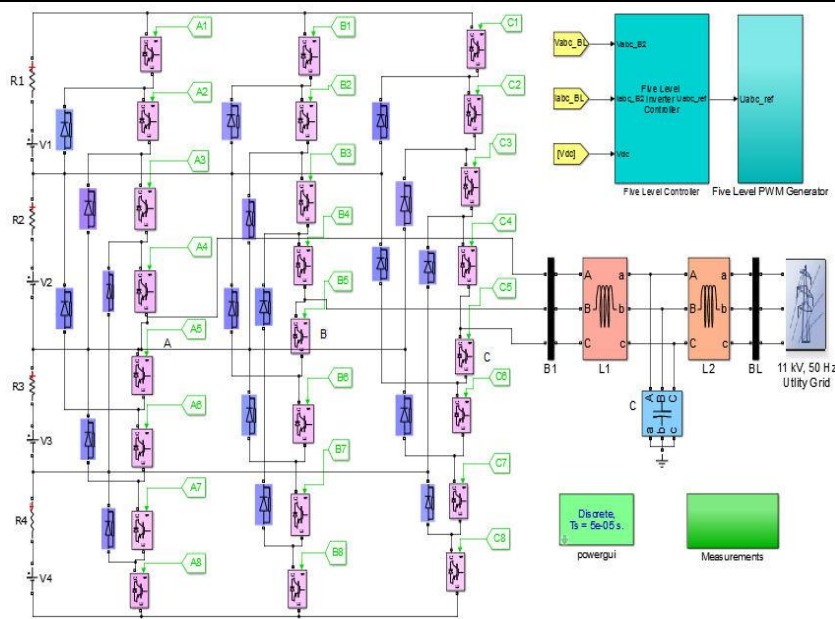


Fig.7 Simulation Model of Grid Connected Three-Phase Five-Level DCMLI

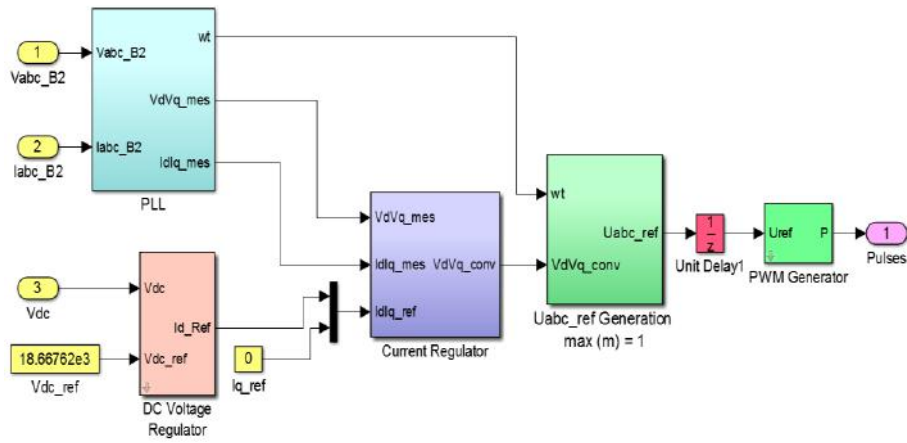


Fig.8 Simulation Model of Control System for Three-Phase Five-Level DCMLI

5. RESULTS AND DISCUSSION

The three-phase five-level DCMLI generates three-phase voltages and currents which are sinusoidal and balance. From the simulation model in Fig.7, the output line voltages and currents from the proposed inverter are shown in Fig.9(a) and Fig.9(b), respectively. These line voltages and currents are un-filtering. After reducing high frequency harmonics by passing through the LCL filter, these voltages will be shaved as sinusoidal waveform.

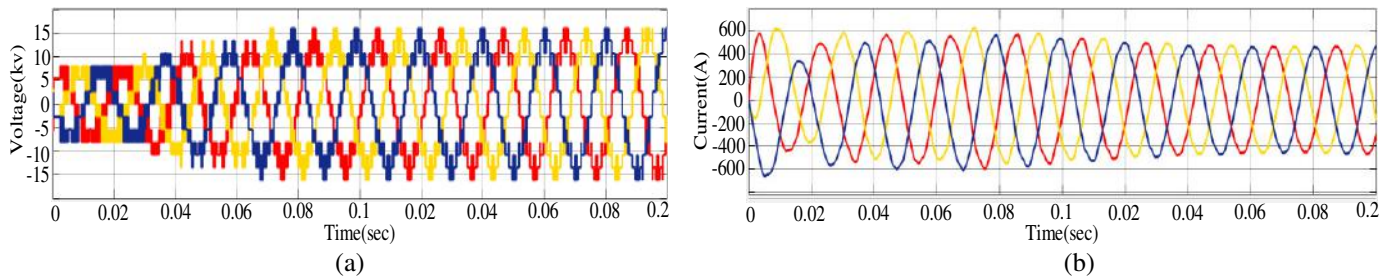


Fig.9(a) Output Voltage Waveforms and (b) Current Waveforms for Three-Phase Five-Level DCMLI

From the simulation result, line voltage and current waveforms at PCC that flow from inverter to grid are shown in Fig.10(a) and Fig.10(b). It can be observed that it has low harmonics distortion. The percentage of harmonic contents is that the comparing to its fundamental frequency content at 50 Hz. The THD values of the voltage and current waveforms are shown in Fig.11(a) and Fig.11(b), respectively. The THD value of the grid current is approximately 0.50%. This value is smaller than 5% which is the recommendation of the IEEE Std. 929-2000.

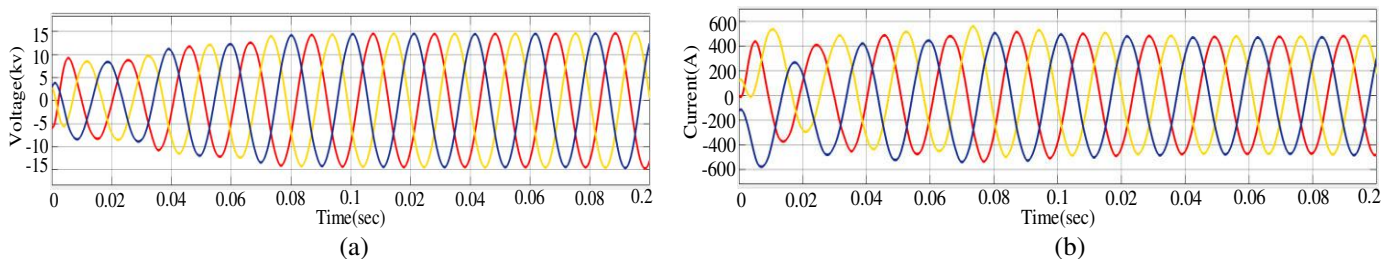


Fig.10(a) Line to Line Voltage Waveforms and (b) Current Waveforms flow from DCMLI to AC Grid

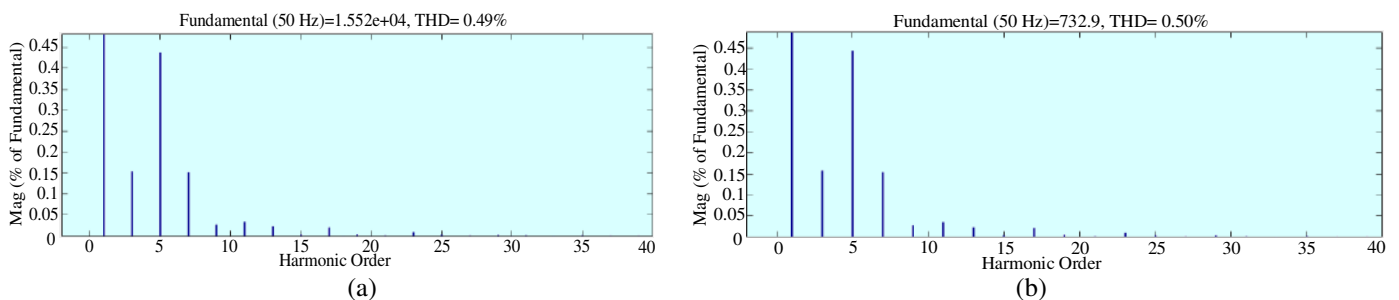


Fig.11(a) FFT plot of Line Voltage Waveform and (b) FFT plot of Current Waveform flows from DCMLI to AC Grid

Fig.12(a) and Fig.12(b) also show the active power and reactive power injected into the AC grid and TABLE III represents the output result values of grid connected three-phase five-level DCMLI.

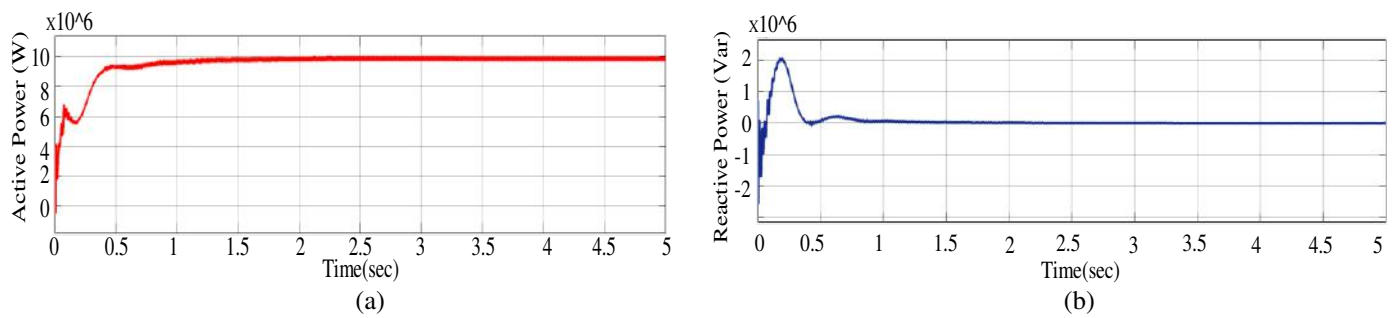


Fig.12(a) Active Power and (b) Reactive Power Received by the AC Grid

TABLE II
 Output Result Values of Grid Connected Three-Phase Five-Level DCMLI

Parameters	Output Result Values
Actual DC-Link Voltage (V_{dc})	18.66762 kV
Reference DC-Link Voltage (V_{dc})	18.66762 kV
Reference d Component of Grid Current (I_d^*)	1.5 pu
d Component of Grid Current (I_d)	0.9935 pu
d Component of Grid Voltage (V_d)	0.6694 pu
Reference q Component of Grid Current (I_q^*)	0 pu
q Component of Grid Current (I_q)	-0.001276 pu
q Component of Grid Voltage (V_q)	-0.001294 pu
d Component Voltage sensed to the Inverter (V_d')	2 pu
q Component Voltage sensed to the Inverter (V_q')	2 pu
RMS Line Voltage Injected into Grid ($V_{ll(rms)}$)	10.97 kV
THD value of Line Voltage Injected into Grid	0.49 %
Current Injected into Grid ($I_{(rms)}$)	517.4 A
THD value of Current Injected into Grid	0.50 %
Active Power Injected into Grid (P)	9.97 MW
Reactive Power Injected into Grid (Q)	-0.0046 MVar

6. CONCLUSION:

In order to construct a grid connected renewable energy system, a number of parameters have to be taking into account and to be optimized in order to achieve maximum power generation. In addition to that a controller has to be used in order to achieve the synchronization to the grid and to perform the power management between the system and electrical grid. The proposed grid connected three-phase five-level DCMLI has a mandated power rating on 10 MW, 11 kV at PCC and 18.66762 kV at DC-link. The proposed carrier-based SPWM technique provides a better performance of voltage and grid current waveform at the PCC. However, LCL filter is also associated to ensures the sinusoidal waveform of both voltage and current. By adjustment of PI controller in the control scheme, the energy can be transferred from inverter. Multilevel inverters are very useful in high power and power quality application. Modulation method are getting trend on multilevel inverter for better performance. The DCMLIs are very beneficial as the number of switches in inverter increases, the harmonics distortion in AC output voltage and current decreases. It also provides reactive power compensation to the AC grid and reduction in electromagnetic emissions because they operate on lower switching frequency. A high number of inverter levels means that the output filter sizes can be minimized and it allows for the possibility of direct connection to the medium or high voltage network. This direct connection leads to the elimination of heavy, bulky, lossy and costly transformers from the system. Moreover, this study shows that the proposed control scheme offers a simple way to study the performance for utility interface

applications. It is simple to implement and capable of producing stationary sinusoidal current and voltage waveforms. It is concluded that the DCMLI is the most feasible inverter for direct grid connection of renewable energy systems.

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